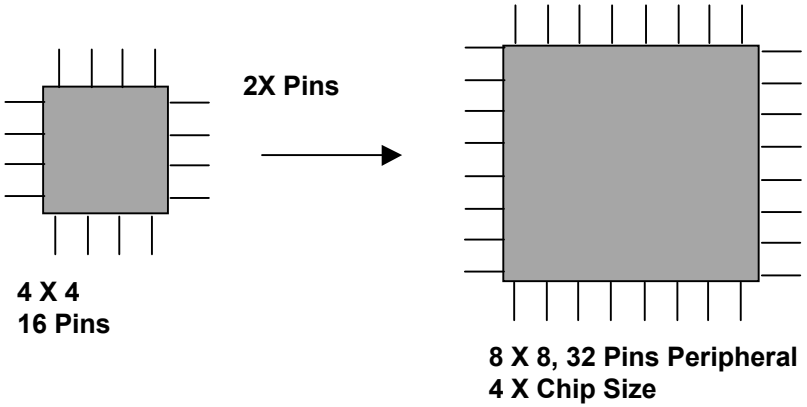
# Temporary Support Systems to Enable Thin Wafer Handling During Grinding, Backside Processing, and Laser Dicing

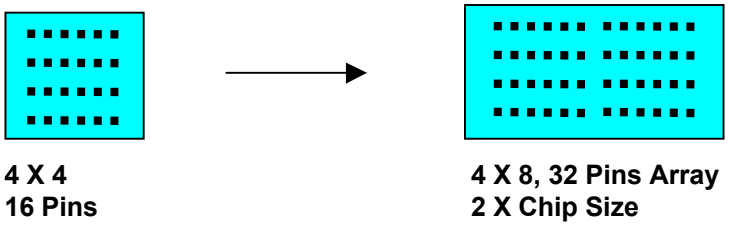
John Moore, Daetec, LLC

October 2009

# 3D Packaging

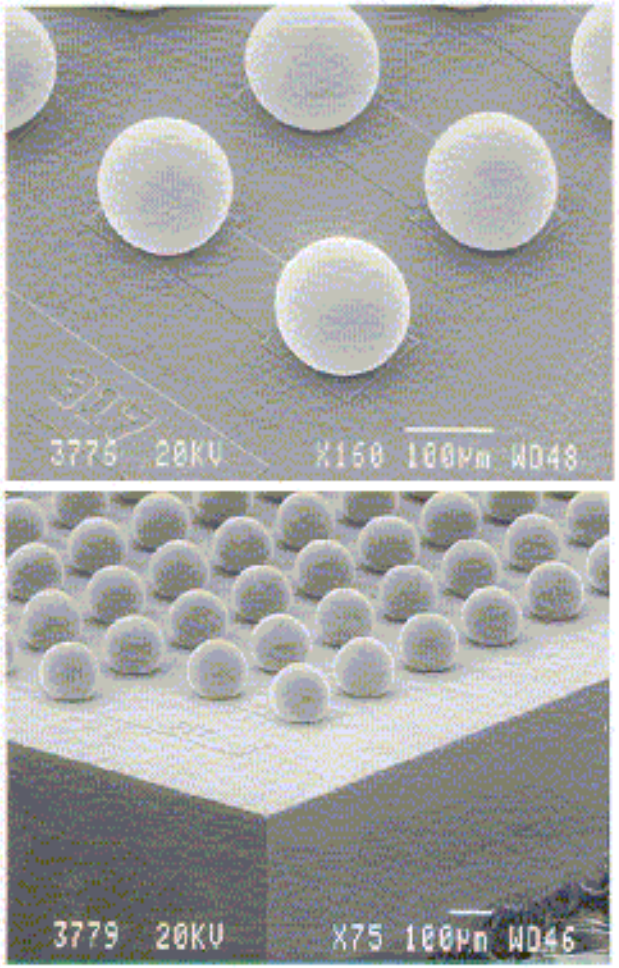
# Wire Bonding vs WLP?



# Flip Chip Process Benefits

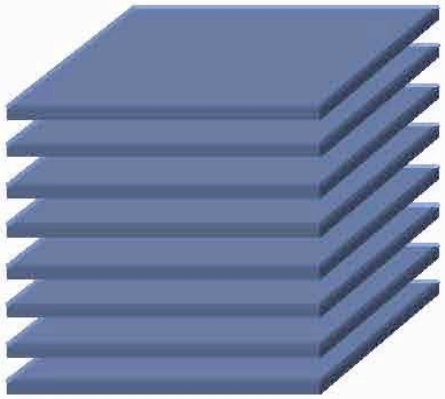
- Device Speed
- Power and Ground Distribution
- Signal integrity
- I/O Density with Area Array
- Lower impedance interconnection
- Package Size / Form Factor
- Low Stress Over Active Area
- Proven Reliability



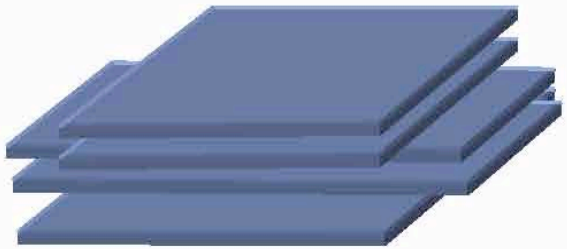

**[Courtesy - Flip Chip, LLC (AZ)]**

# 3D assembly of integrated circuits

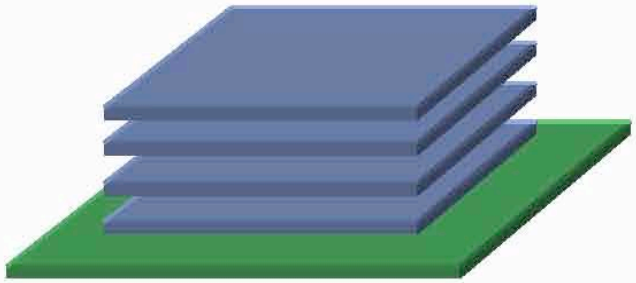
- Higher integration density by stacking die, e.g:



Homogeneous Memory Stack



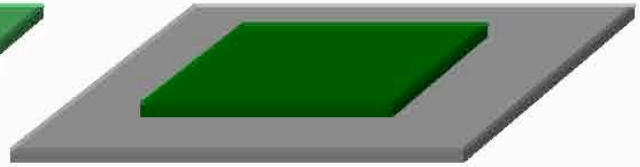
Heterogeneous Memory Stack



Microprocessor & Memory Stack

Digital CMOS + analog/rf chip

Digital CMOS + Sensor/MEMS chip



IC or IC stack

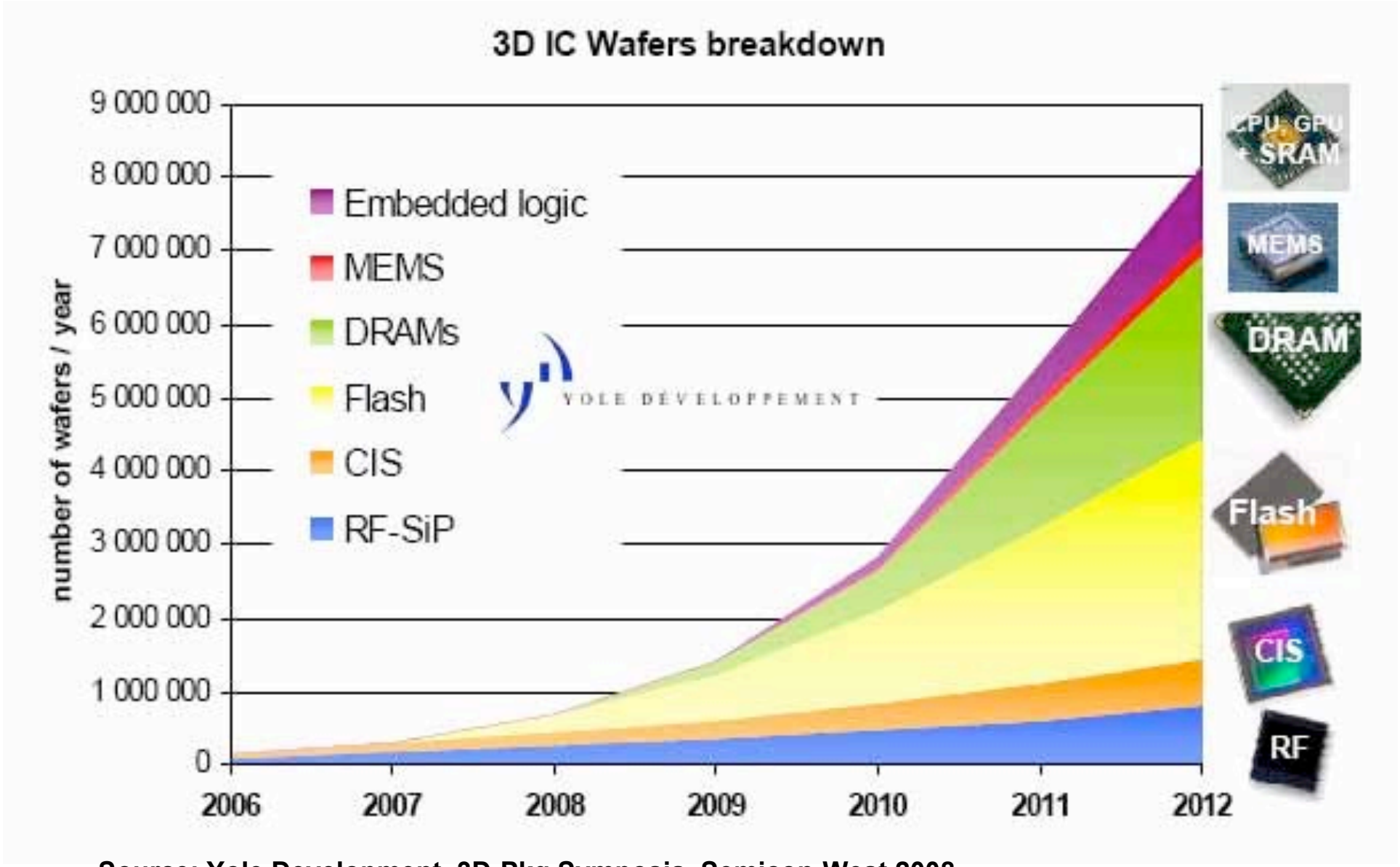
On Si-interposer or IPD substrate

- Interconnectivity: at bond-pad level

# Market

- 3D-Plus (F)
- All-via (US)
- Amkor (Kr, USA)
- ASAT (China)
- ASE (Taiwan)
- ASET (Taiwan)
- ASM International (NL)
- E2V (F)
- EVG (AT)
- Casio Micronics (JP)
- Chipbond (TW)
- Cubic Wafer (USA)
- EM Microelectronics (CH)
- Flip Chip International (USA)
- Form Factor (USA)
- Fraunhofer IZM (G)
- Freescale (F, G)
- Fujikura (JP)
- Fujitsu (JP)
- Hitachi (JP)
- Honeywell Specialities (USA)
- Hymite (Dk)
- Hynix Semiconductor (K)
- IBM (USA)
- IMEC (B)
- Infineon (G)
- Intel (US)
- Leti (F)
- LSI Logic (USA)
- MagnaChip (K)
- Matsushita Electric Works (JP)
- Micron (Singapore)
- µresist (G)
- National Semi (USA)
- NEC (J)
- Nokia (FIN)
- Oki Electric (JP)
- Philips Semiconductors (NL)
- Rensselaer Polytechnic Institut
- Samsung (Kr)
- Sanyo (JP)
- Schott (G)
- Seiko Epson (JP)
- SEMITOOL (USA)
- Silex (SW)
- SMIC (Shangai)
- SPIL (Taiwan)
- STATSChipPac (USA)
- STMicroelectronics (France)
- SÜSS microtec (G)
- Synova (CH)
- Tessera (IS/US),
- Texas Instruments (US)
- Tezzaron (USA)
- Toshiba (JP)
- TSMC (TW)
- VTI Technologies (Fi)
- VTT Technology (FIN)
- Xintec (Taiwan)
- Ziptronix (USA)
- Zycube (J)

**Source: Yole Development**




**Source: Yole Development, 3D-Pkg Symposia, Semicon-West 2008**

# Bonders w/Modular Flexibility

SÜSS MicroTec

**CBC 200**

***Automated***

**XBC 300**

***Semi-Automated***

**CB8**

**Source: Daetec, LLC, 3D-Pkg Symposia, Semicon-West 2009**

# Market Size

- Total: ~$4b
- Materials: $0.63b
- Equipment: $1.3b
- Services: $2b

- **Source: 3D-Pkg Symposia, Semicon-West 2009**

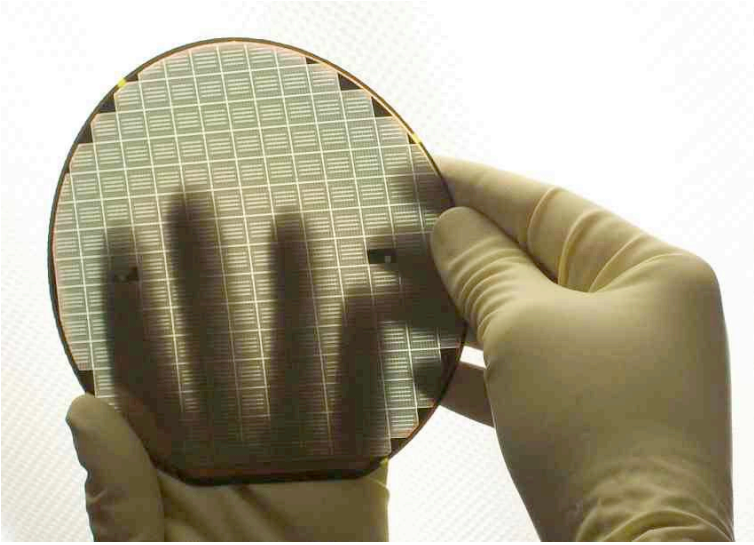
# Thin Wafer Handling

# What is Wafer Thinning?

- Thermal management by substrate removal
- Reduce thickness @ 700um to <25um
- >20yrs commonly by chem etch to <250um
- Current practice is grinding followed by stress relief etching - wafers with completed devices
- Backside processing follows thinning
- Mandatory with high power chips (e.g. GaAs)
- Silicon at 300mm is emerging

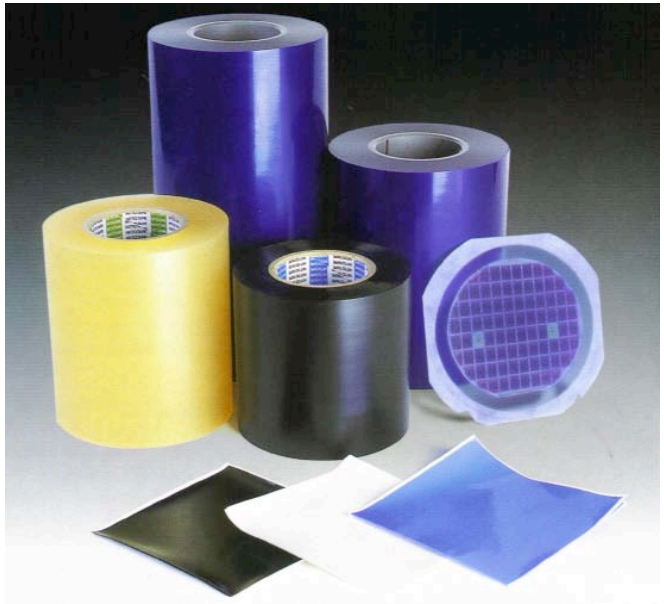
# Typical Wafer Handling Means

- Tape
- Corresponding Wafer
- Chuck
- Carrier & Adhesive



# Tape Contact

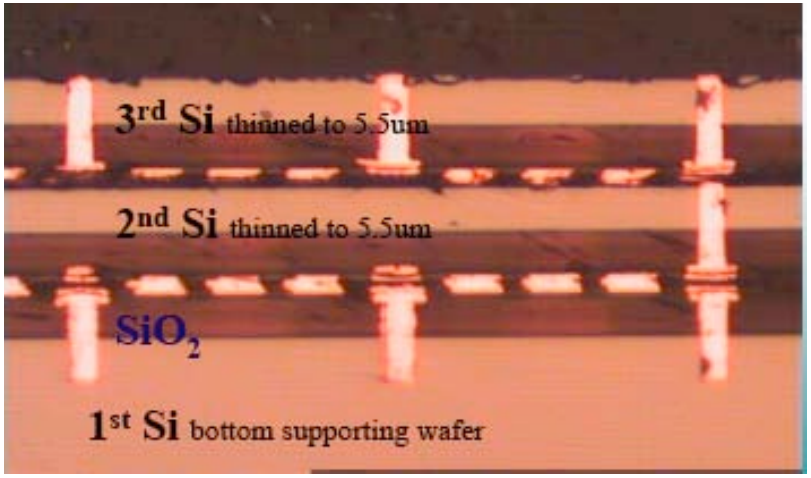
- Simple
- Inexpensive
- Grind/etch to <50um
- Limited chem/therm resistance
- Removal may be tricky (heat or UV)



**Source: SEC as distributor for Nitto-Denko**

# Corresponding Wafer

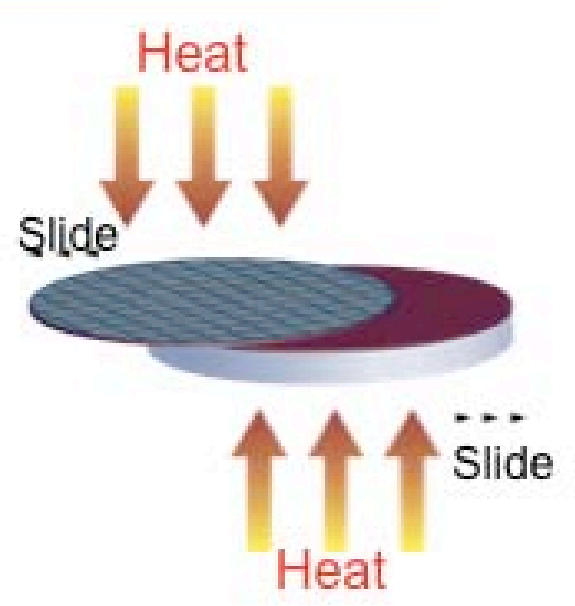
- Cu-to-Cu bonding
- Tool & inspection for ⇑ KGD
- Grind/etch to <10um
- Possible license




**Source: Patti, Tezzaron, 3D PKG Syposia, 2008**

# Chuck

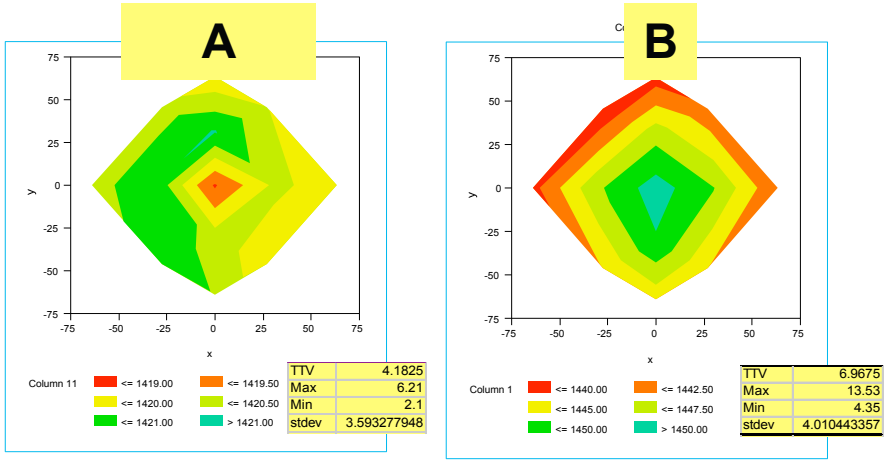
- Vacuum or electrostatic
- Single wafer only
- Temporary only
- Substrate sensitive <50um
- Tool required




**Source: EVG Debonding tool, 3D Pkg Symposia, Semicon 2009**

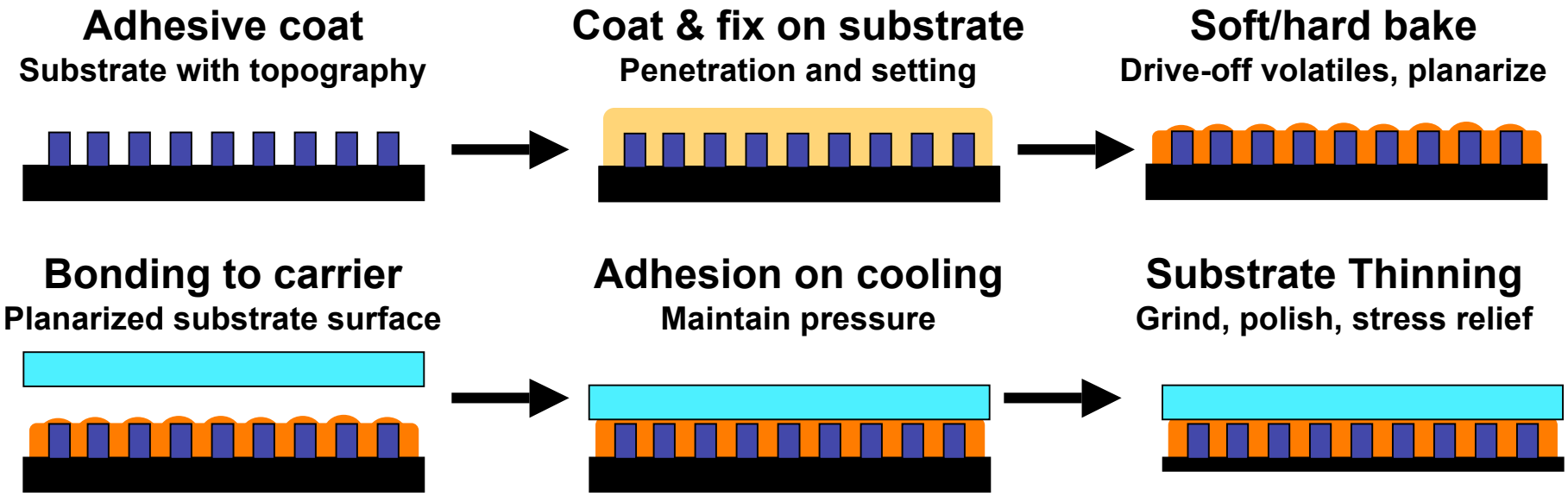
# Carrier & Adhesive

- Several configurations
- Wide range of products
- Temporary
- Therm & Chem resistant
- Stable
- Able to thin <25um
- Production capable
- Inexpensive



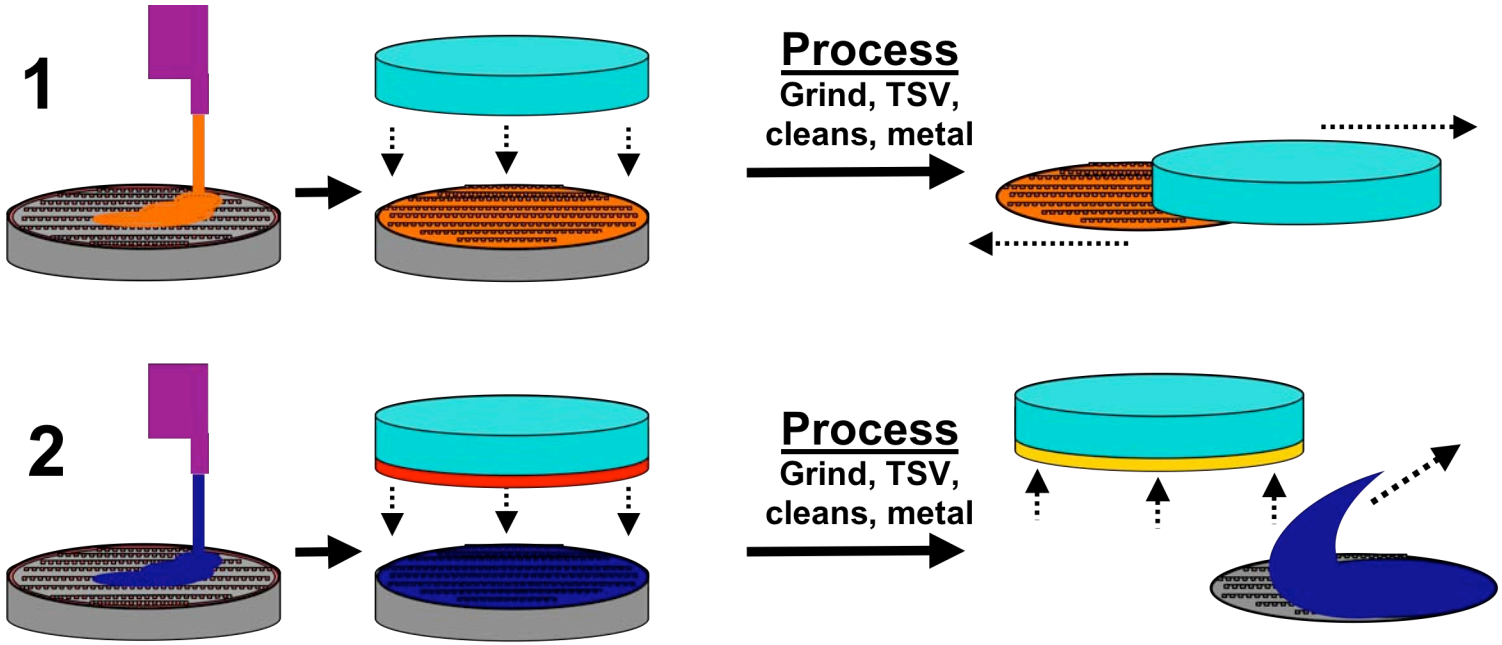
# Adhesive & Carrier

# Thermoplastic Spin-On Adhesive Coating and Mounting Model

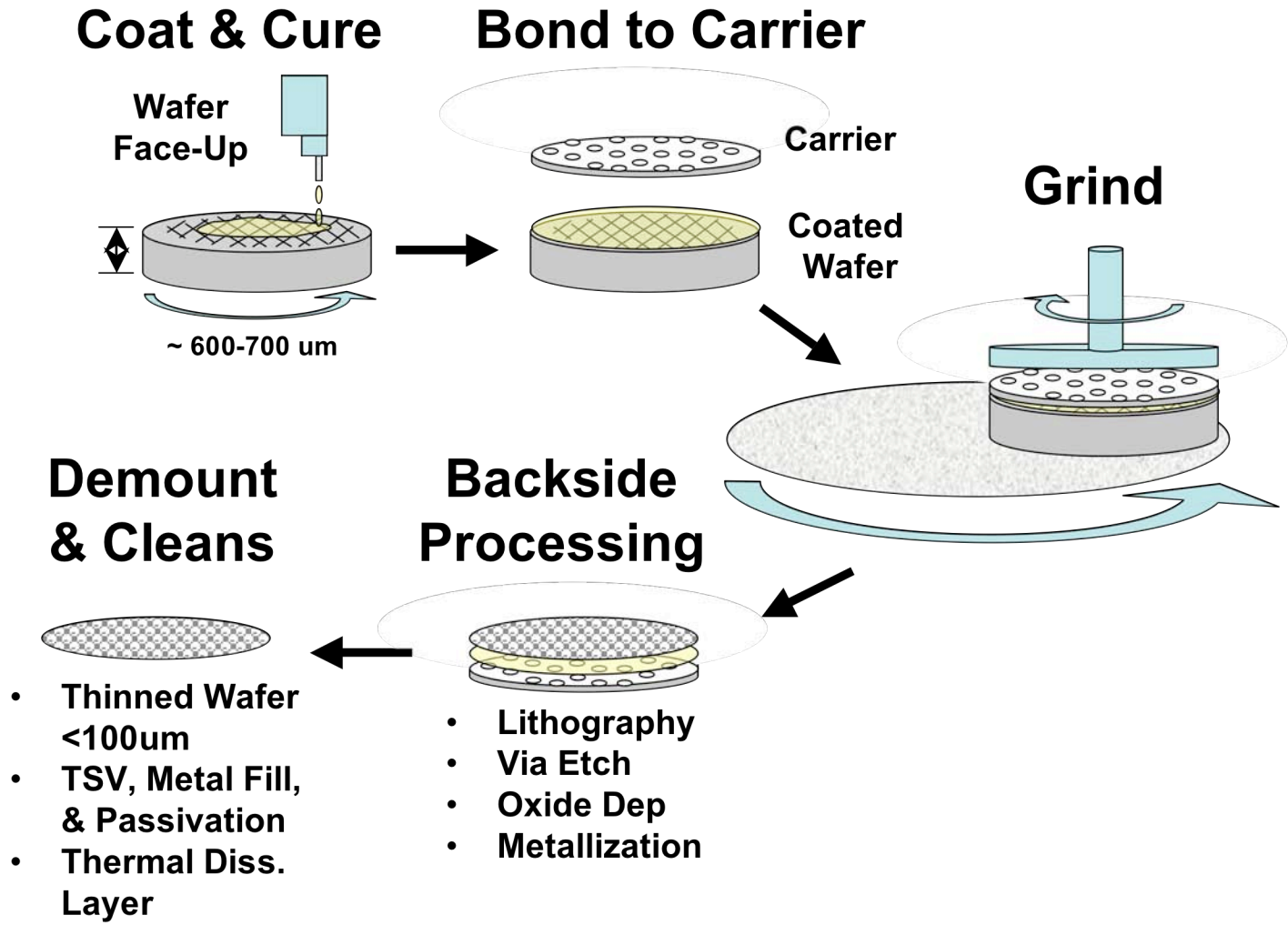


# Commercial Processes

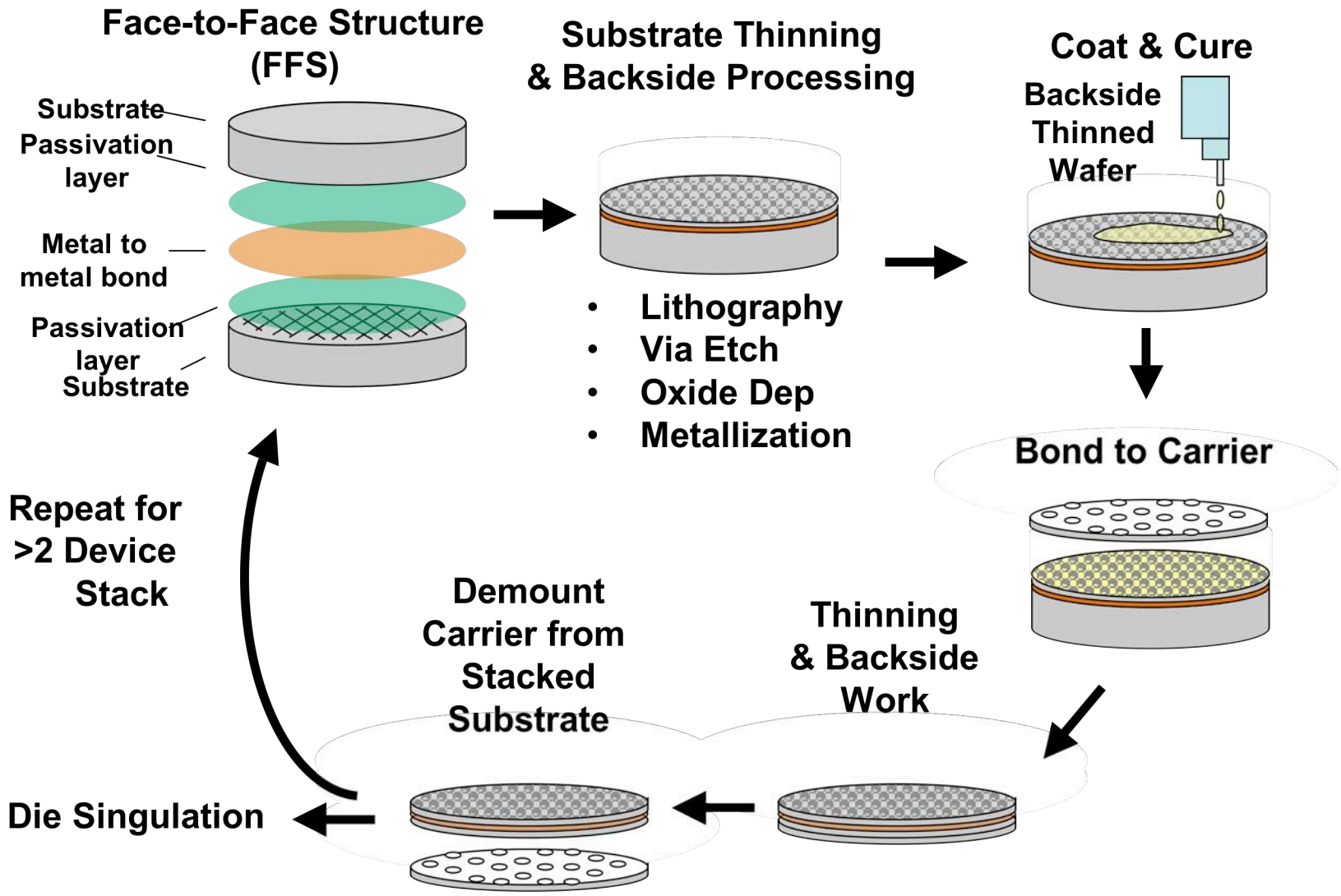
*Two leading processes exist*



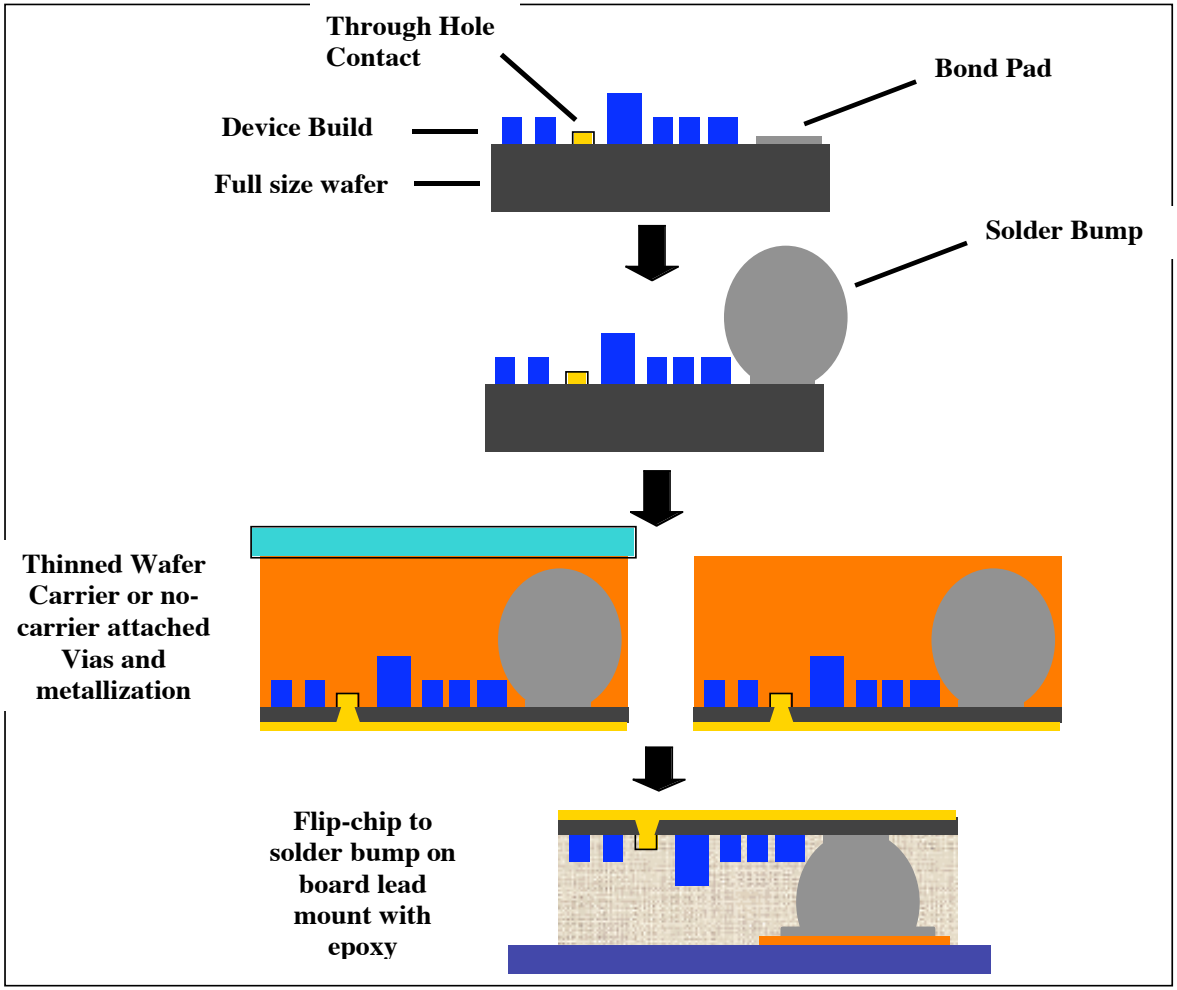
# 3D Packaging Processes



# 3D Packaging Processes



# Adhesive Support for Wafer Bumping Flip Chip Process

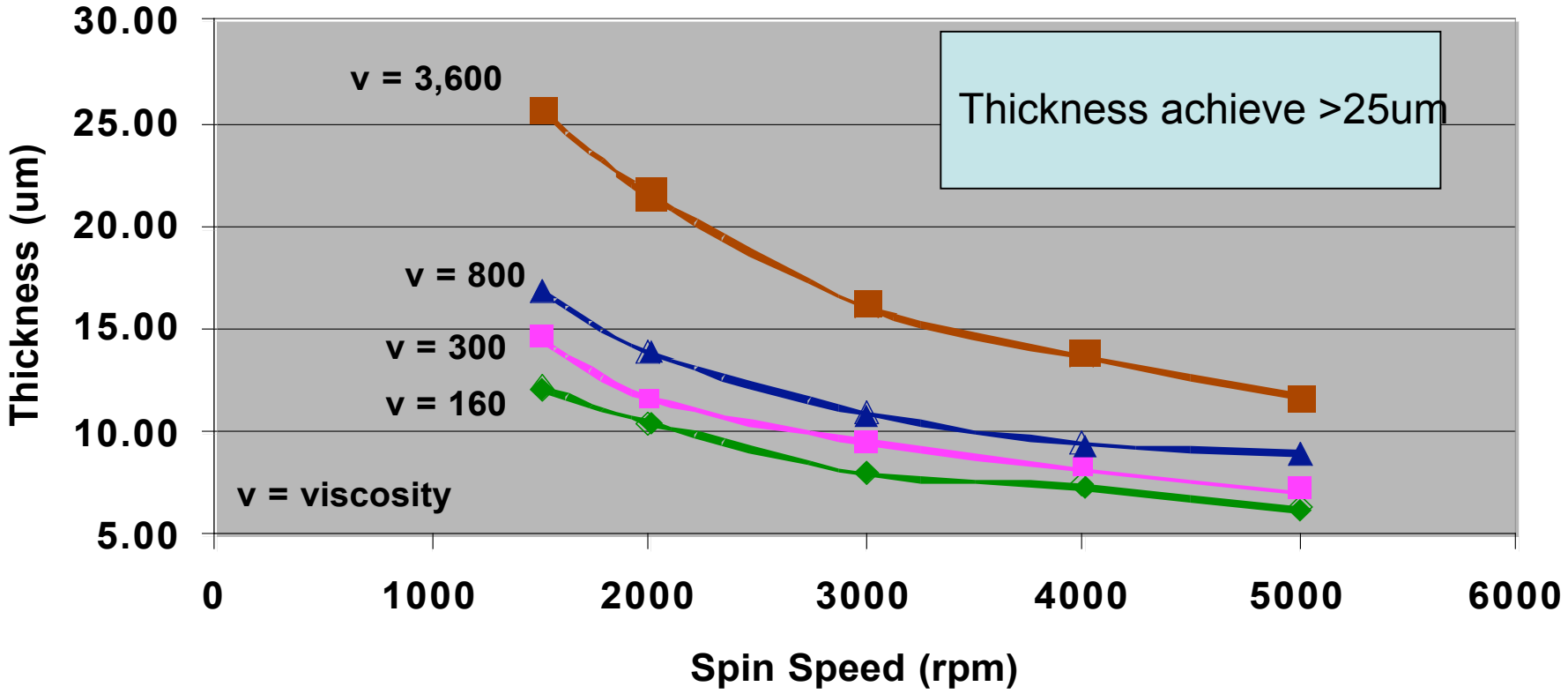


# Adhesive Key Properties

- Consistent thickness
- Uniform
- Thermal resistant
- Low outgas
- Simple removal

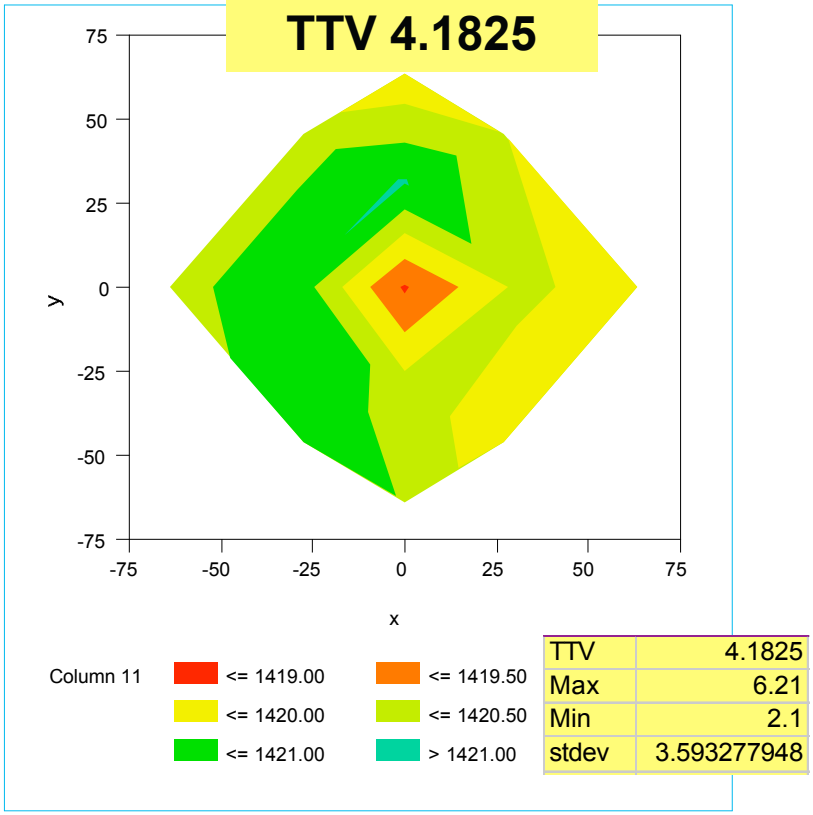
# Coating on Smooth Substrates

## Thickness vs. Spin Speed



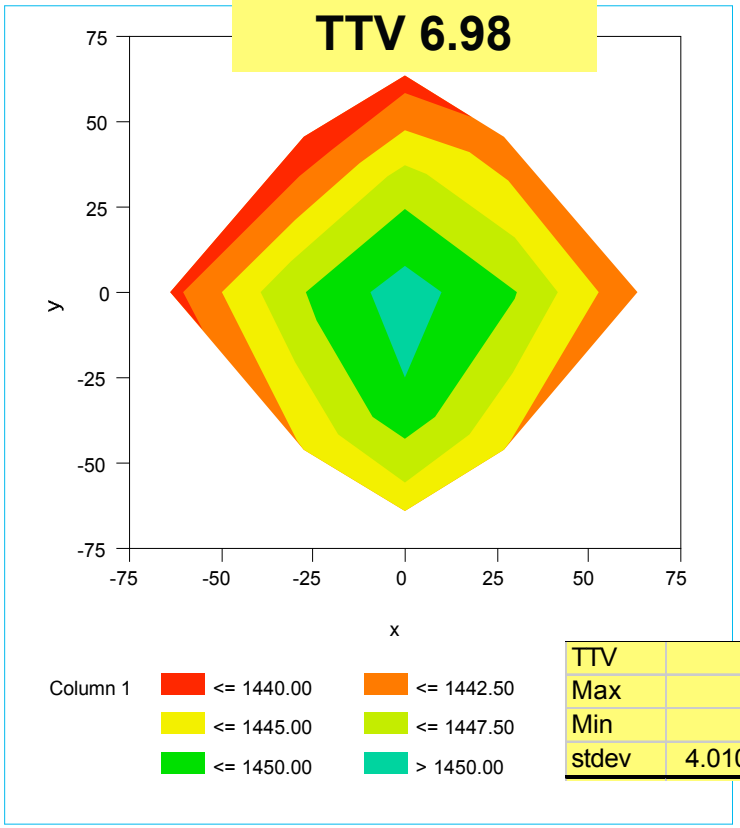
# Pkg TTV - Adhesive Development

**Formulation A**
**TTV 4.1825**




| | |
|---|---|
| TTV | 4.1825 |
| Max | 6.21 |
| Min | 2.1 |
| stdev | 3.593277948 |

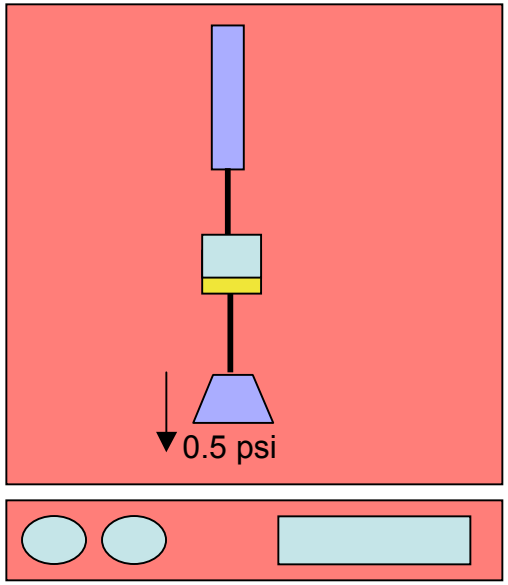
**Formulation B**
**TTV 6.98**



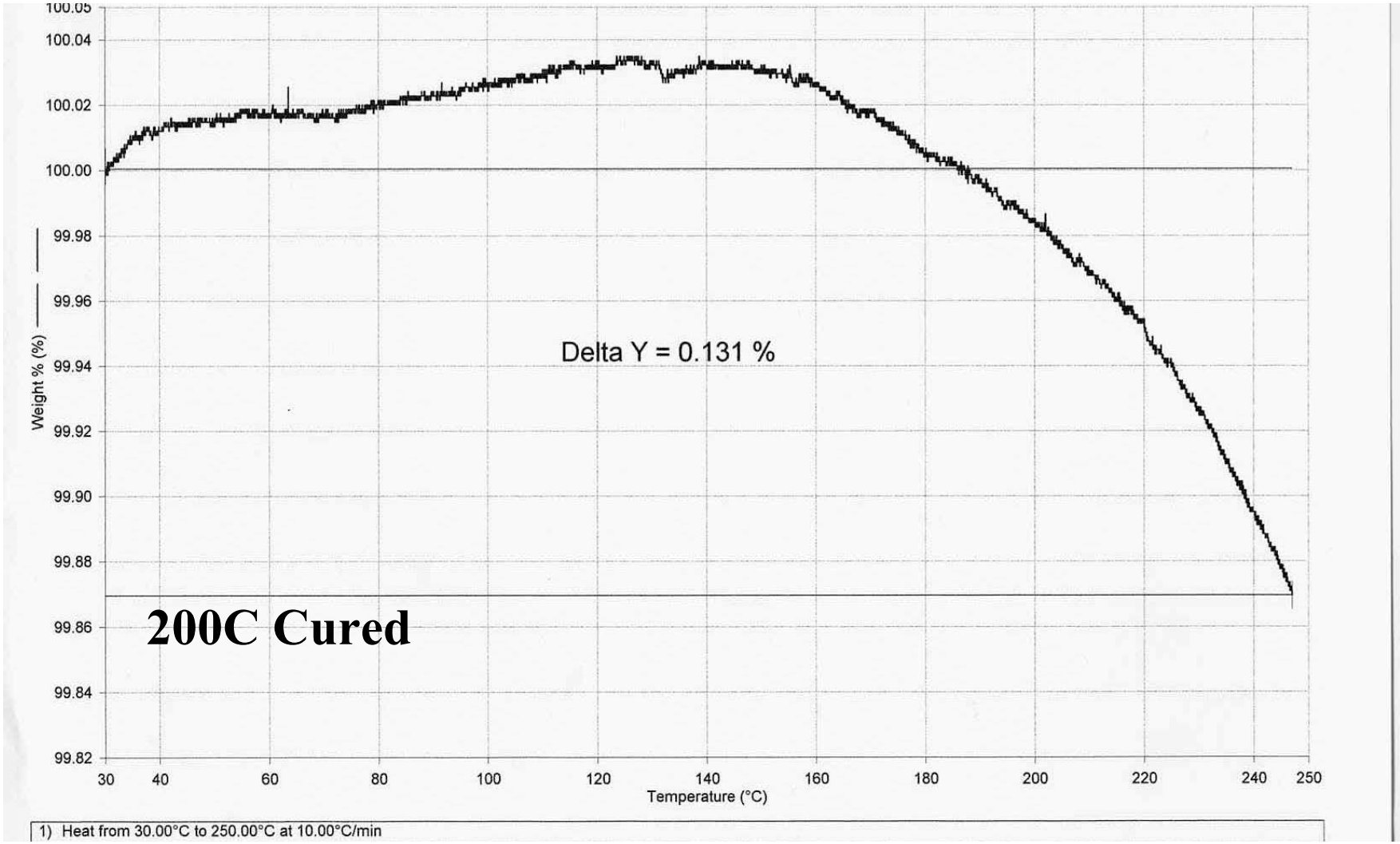

| | |
|---|---|
| TTV | 6.9675 |
| Max | 13.53 |
| Min | 4.35 |
| stdev | 4.010443357 |

# Softening Pt by Thermal Shear

| # | Air temp debond in oven (C) |
|---|---|
| 52 | 118 |
| 23 | 144 |
| 24 | 140 |
| 58 | 125 |
| 59 | 129 |



# Thermal Analysis - Cured



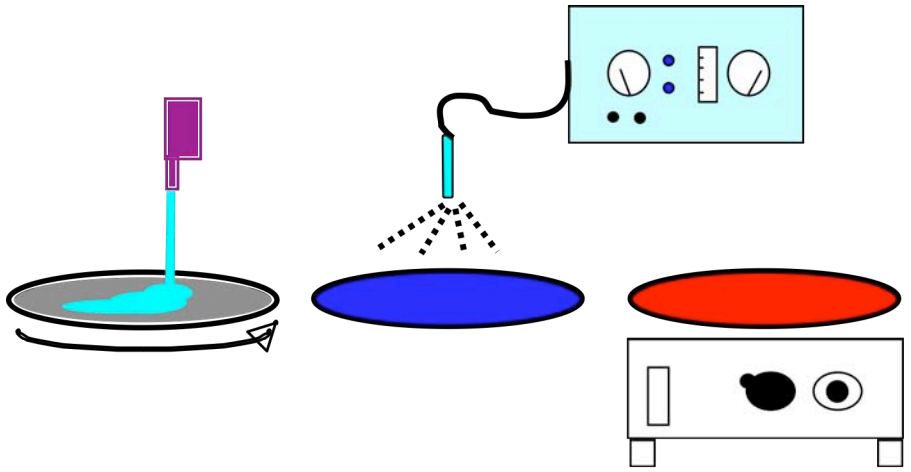
# Encapsulants/Molding

# Die Encapsulant - 3D Pkg

- Thickness >30um, >200um
- Adhesion to a range of substrates
- Thermal resistant
- Simple aqueous cleans

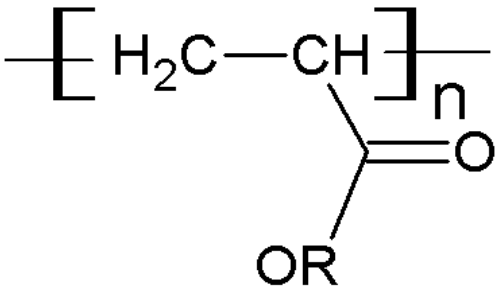
# Acrylic Chemistry

- Similar to negative-tone PRs
- Same initiators as negative PRs
- Same PRs as used in WLP (bumping)
- Exposure similar to PRs



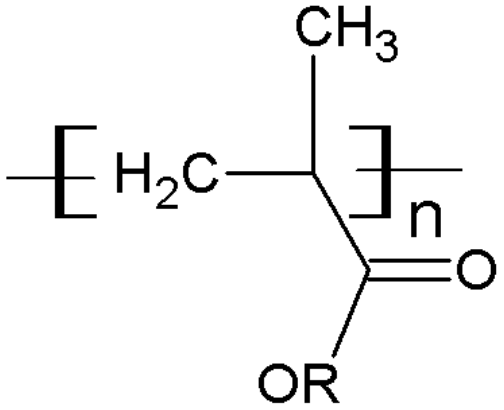
Coat Expose Heat

# Support Chemistry



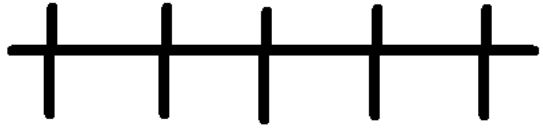

**Polymethylacrylate**

**PMA**

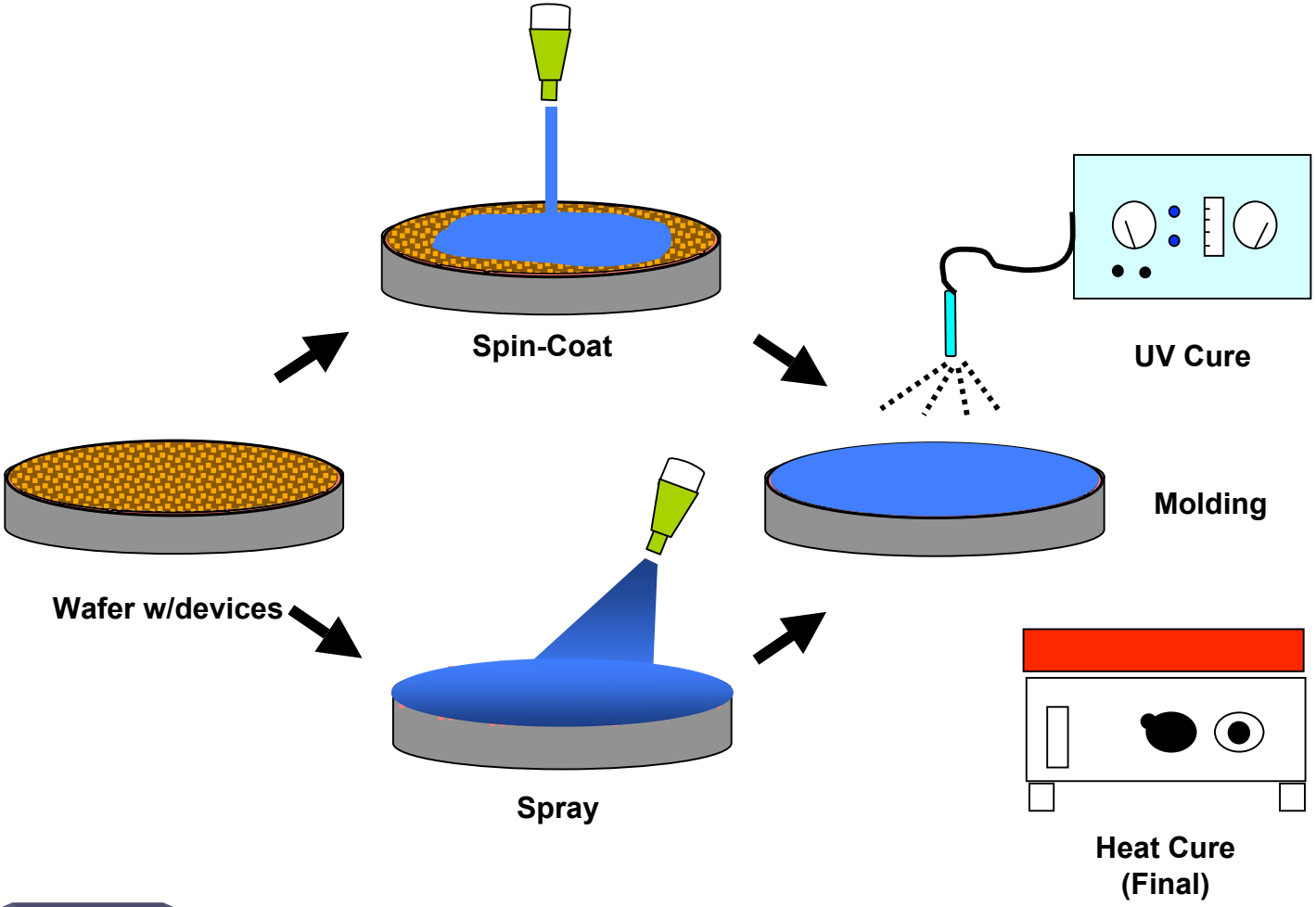



**Polymethylmethacrylate**

**PMMA**

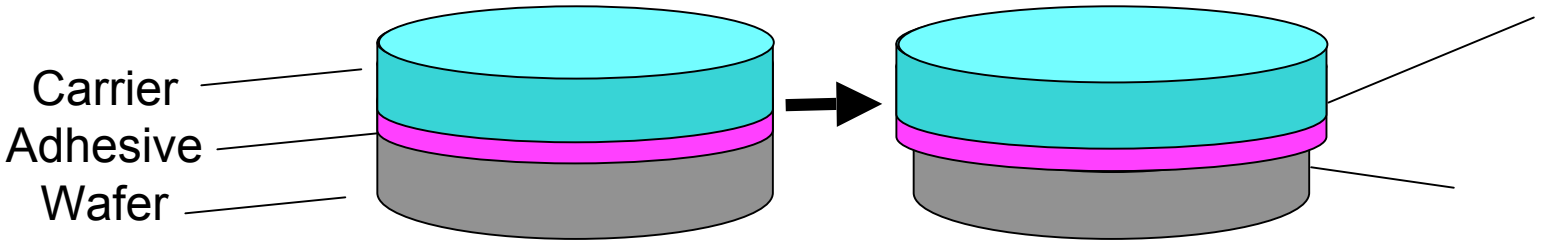


# Process Development



# Edge Protection

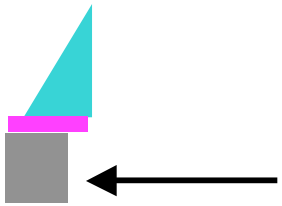
Conventional Stack




Stack

Edge Overlay

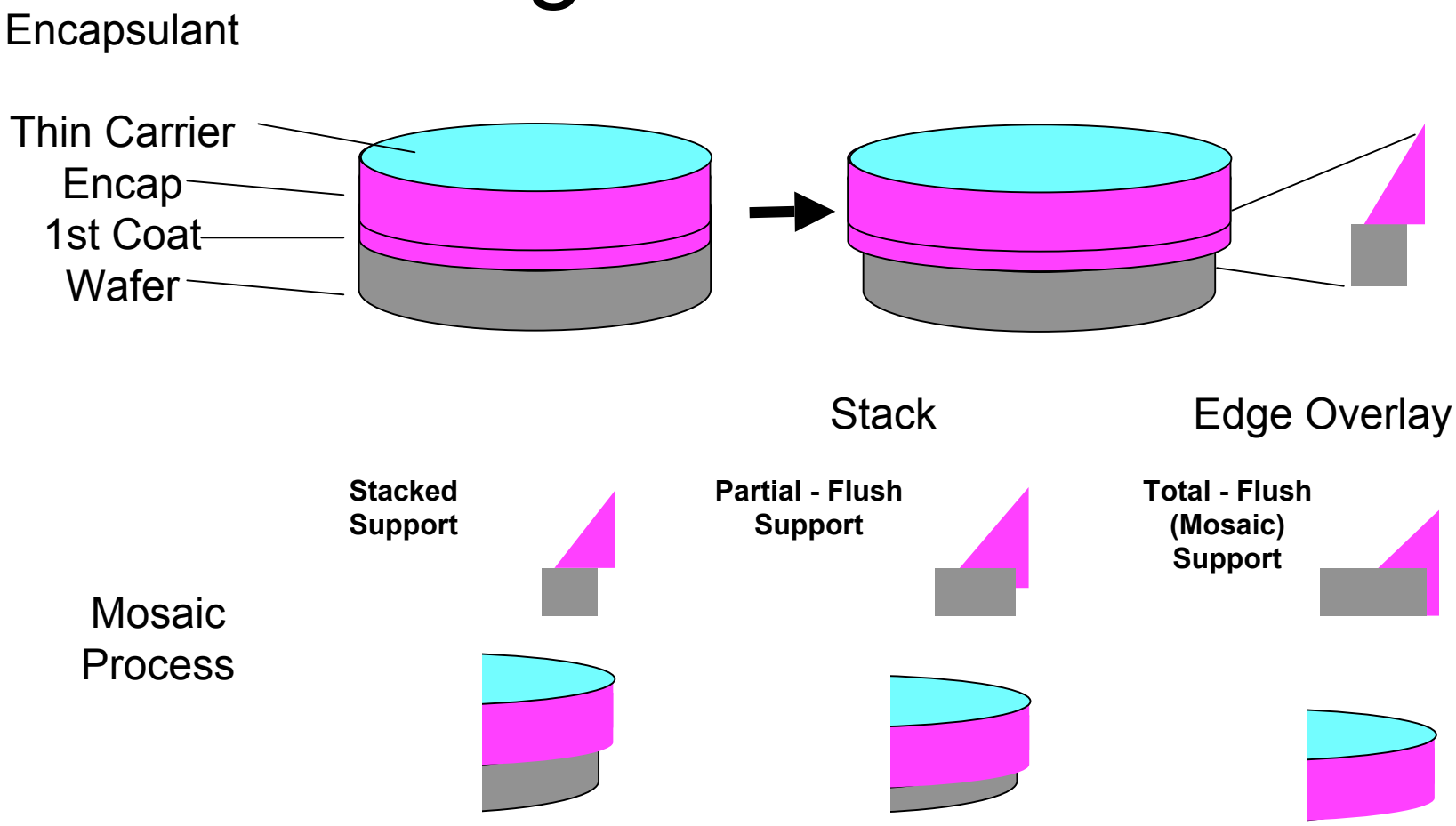
Little/no Edge Protection



Shear Force Grinding

Edge off grinding

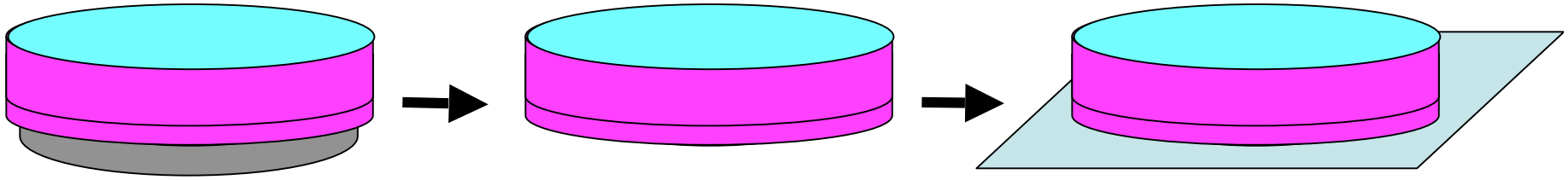
# Edge Protection



# Encap Highlights

- Molding process
- Uniform w/carrier attachment
- Stable to high temp, >250C, could be higher
- Large bond line access for cleans
- Aqueous cleans

# Process to Tape

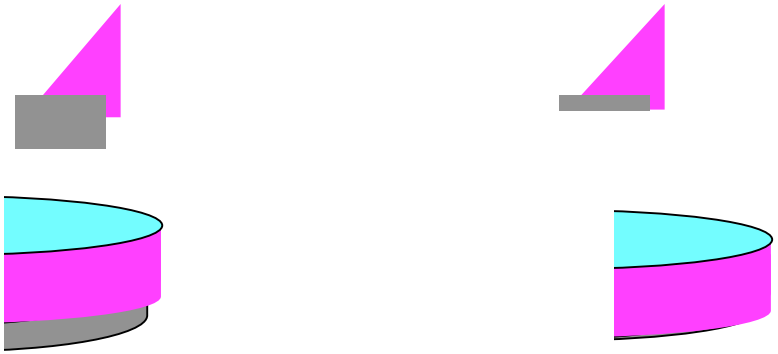


Stack

Thinned wafer

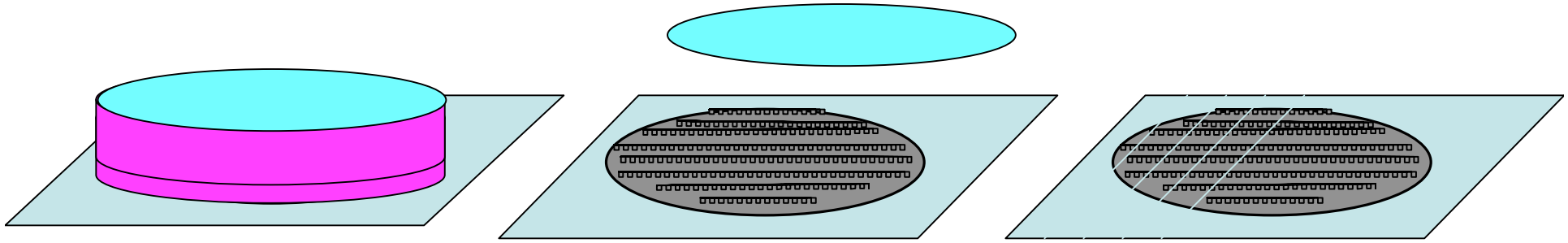
Tape Attachment

**Partial - Flush Support**



Prepare for Cleans

# Process to Dicing



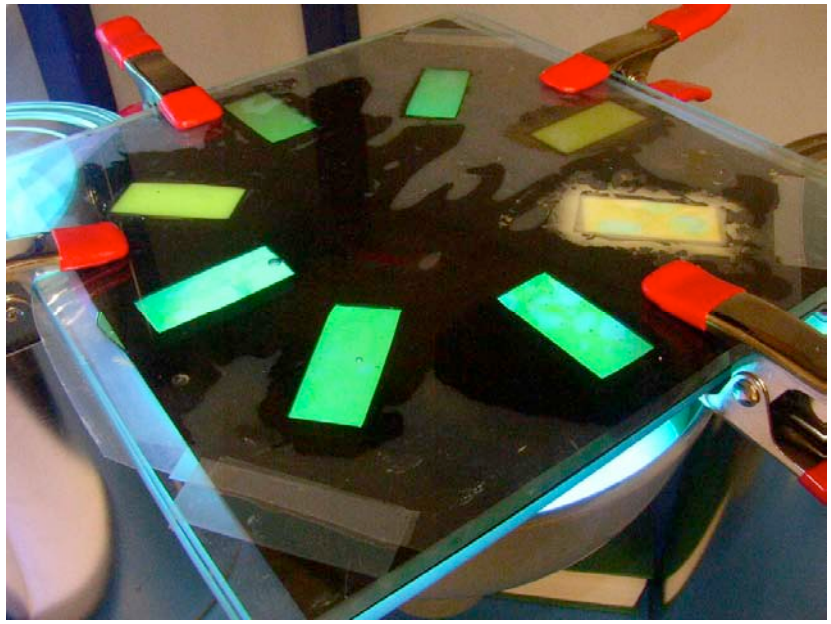
Tape Attachment

Aqueous Cleans
Safe for Tape

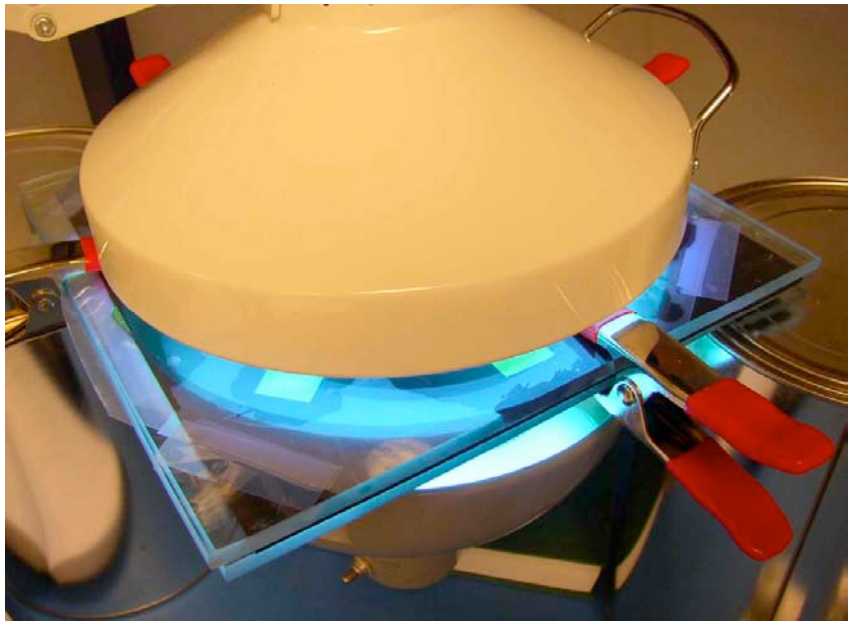
Release carrier
For recycle

Dicing

# Encapsulation Process



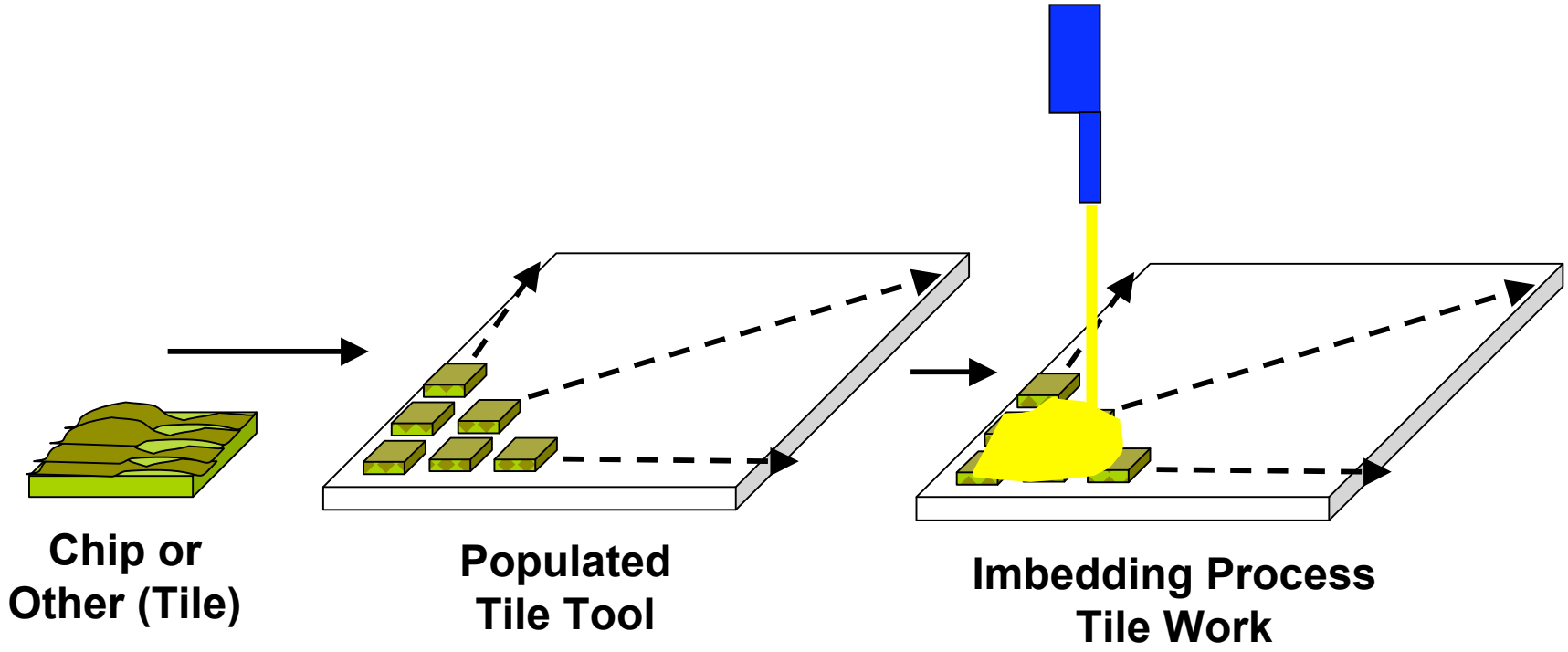
Molding - bottom exposure



Molding - top & bottom exposure

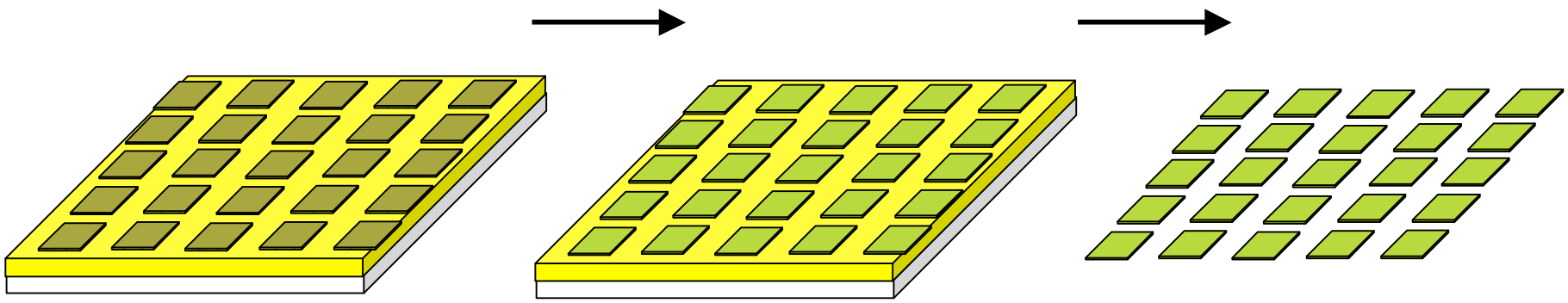
# Mosaic

# Mosaic (Chip Thinning)

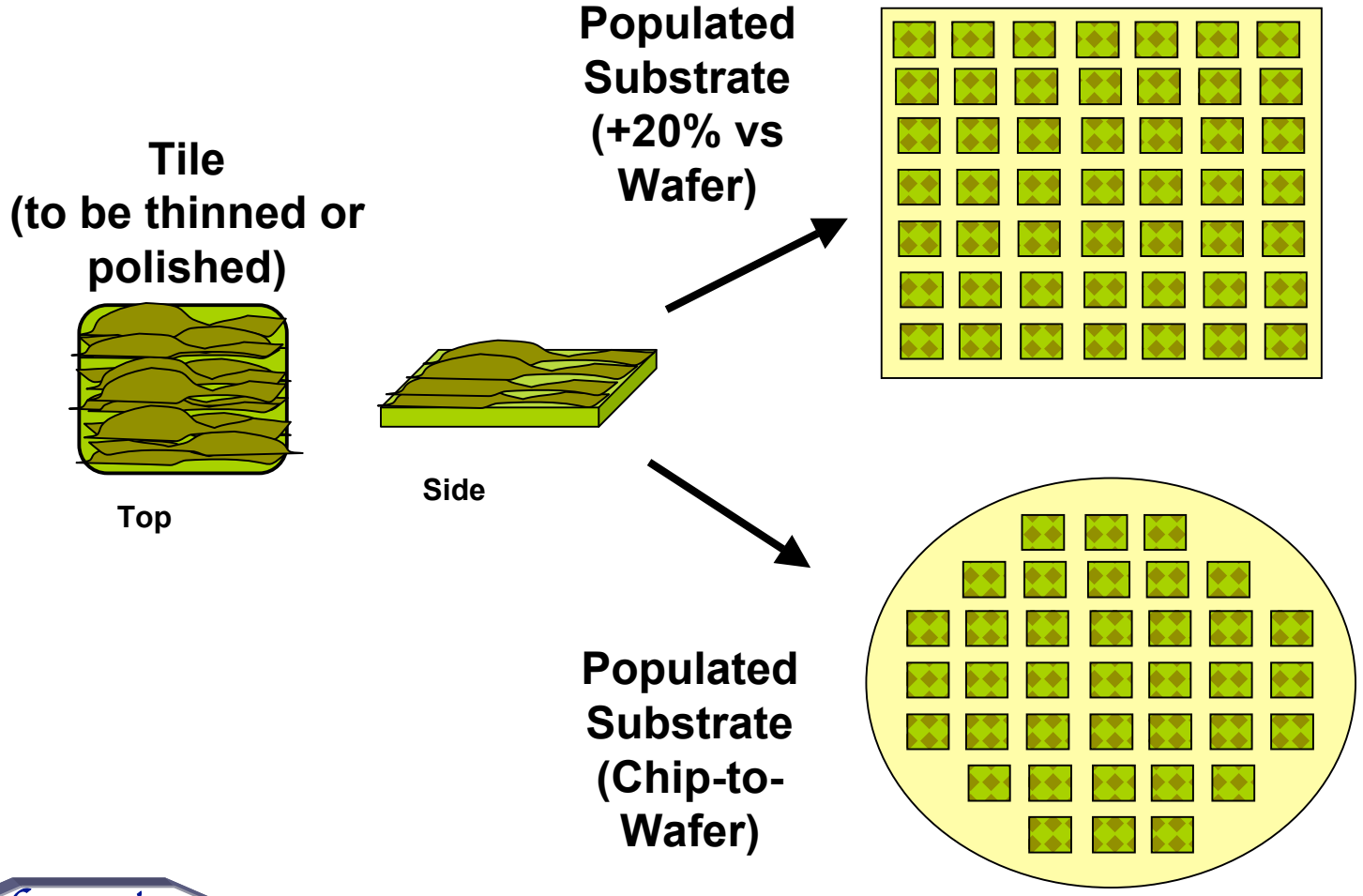


# Mosaic

**Embedded Tiles** → **Grind & Polish** → **Tile Release (Cleans)**

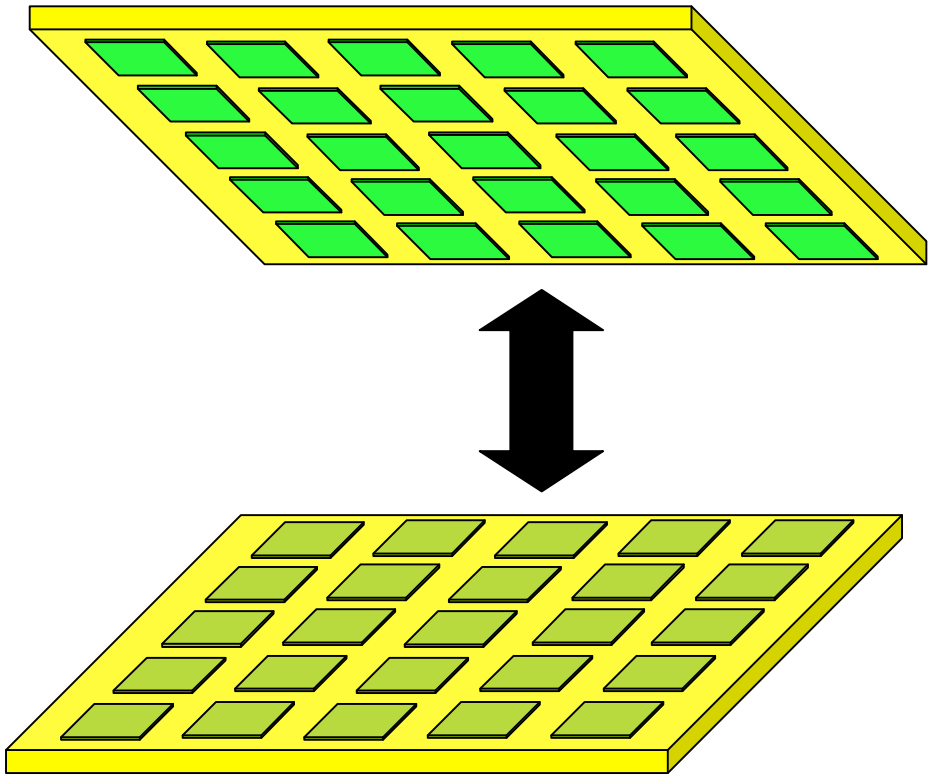


# Mosaic


Tile
(to be thinned or polished)
Top
Side
Populated Substrate (+20% vs Wafer)
Populated Substrate (Chip-to-Wafer)

# Mosaic

**Mosaic may be ground and polished on one or both sides. Once the mosaic is completed, it becomes a handling exercise. Offering polishing to either side of the mosaic provides needed process flexibility.**



# Summary

- Thinning is an important part of 3D Pkg
- Key processes use adhesives & carrier
- Polymers must meet desired properties
- Encap (molding) provides benefits for thin wafer handling
- Aqueous soluble may use tape-transfer
- Tape-transfer proceeds to rapid dicing

# Contact for More Information

- DAETEC develops new products and processes to solve manufacturing problems and introduce new ways of doing business.
- Diversified Applications Engineering Technologies (DAETEC)

  Camarillo, CA (USA) (805) 484-5546

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