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Back-side Processing of GaAs Wafers

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Abstract. Back-side processing of GaAs wafers includes all the manufacturing process steps from just after final front-side electrical test through die separation and packaging. The back-side process flow of a typical GaAs Fab can be separated into two major branches. The first branch is for GaAs die that do not require back-side via holes or metal. The main process steps involved are wafer thinning, dicing, die inspecting, and packaging. The second branch is for die that require back-side metal and in most cases through substrate via holes. This branch involves several additional process steps including wafer / carrier mount, back-side photoresist mask definition, via hole etch, photoresist strip, oxygen plasma clean, seed layer deposition, and electroplating. This presentation will focus on several key back-side process steps that have historically presented problems and discuss some of the recently available options that can be implemented to increase yield and throughput.

Introduction

Yield at back-side is crucial to the success of a GaAs Fab as a result of the large investment already made in processing the wafers through front-side. Also, major challenges exist in scaling up from a 4" to 6" diameter wafer platform. Fab equipment vendors over the past few years have taken notice of the growth in demand for GaAs based devices for wireless applications and have started to address some of the tool deficiencies that previously existed at a few of the main back-side process steps. However, the costs of these new tools can be considerable, so Fab process engineers and managers need to carefully review cost of ownership models and future wafer volume requirement estimates in order to justify these capital equipment purchases and installations. The recent decrease in demand for wireless devices illustrates just how challenging these capital equipment purchase decisions can be.

Back-side Process Flows

Detailed reviews of the GaAs wafer back-side process flows have recently been published.[1-3] For 150 mm diameter wafers that do not require vias and back-metal, an ultra-violet (UV) back-grinding (BG) tape is usually used to protect the wafer front-side. The UV BG tape typically consists of a polyolefin base film, an anti-static layer, an acrylic UV curable adhesive layer, and a polyester backing film, which is peeled off just prior to mounting the tape onto the wafer front-side surface. A cross section for Ultron Systems, Inc UV anti-static tape is shown in Figure 1. Other UV BG tape vendors include Furukawa Electric and Lintec (Adwill series). The thickness of the polyolefin base film can range from 70 to 250 μm and serves as a support for the thinned wafer. The combined thickness of the adhesive and anti-static layers typically ranges from 18 to 40 μm, and the total thickness variation of the tape is usually within ±6 μm. If the wafers have air-bridges, a thick photoresist can be applied to protect the air-bridges during the tape mount and subsequent thinning steps.

For high volume manufacturing, an automatic wafer taper and de-taper are typically used.[4] Automatic taper and de-taper vendors include Takatori, Microcontrol, Teikoku (Okamoto), Lintec (Adwill series), and Nitto Denko. The de-taper can be purchased with a UV exposure module option. Upon UV exposure the adhesive layer strength of the tape is reduced to 1-5%.[4] The UV BG de-tape step should be done after the thinned wafers have been mounted on dice tape frames, so that thinned wafers are continuously supported by tape base film from the grind through dice steps. Wafer tape system vendors are developing new automated tools that combine the UV BG de-tape step with the dice tape frame mount step that are targeted for Smart Card applications.[5] Hopefully, these new tools will soon be available for use on 150 mm diameter GaAs wafers. A few GaAs Fabs have demonstrated that 150 mm wafers with UV BG tape are thinned to a target thickness range of 250 to 125 μm with high yield.

An automated single wafer / dual spindle grinder is used to perform most of the wafer thinning followed by a post grind wet etch or polish to remove the grinding damage layer.[2, 3] The dual spindle grinder performs a fast, bulk, rough grind followed by a slow, thin, fine grind to achieve high throughput and minimize the thickness of the grinding damage layer. Dual spindle / single wafer grinder vendors include Strasbaugh, Disco, Okamoto, and G&N. Okamoto also offers a post grind wet etch module option for grinding damage removal.

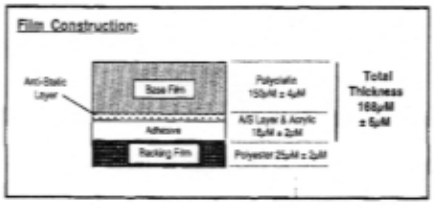


Figure 1: UV tape cross section for Ultron Systems, Inc. P/N 1043

For 100 mm diameter GaAs wafers, a 10-12 μm thick photoresist layer can be used instead of tape to protect the wafer front-side. However, handling and breakage become issues if the wafer is thinned below 150 μm since it is unsupported between the thinning and dice tape fame mount steps.

For wafers that require vias and back-metal, the wafers may be thinned between 100 and 20 μm, which requires that the wafer be mounted on a carrier using a high

temperature wax or thermoplastic adhesive.[2, 6, 7] Liquid thermoplastic adhesives can be applied using a coat and bake track while dry film adhesives can be applied using a dry film vacuum laminator. Perforated sapphire carriers are currently widely used for 150 mm wafer processing.[2, 3] However, new automated wafer / carrier mount and de-mount tools may allow for the use of non-perforated carriers.[7] Vendors offering these tools include BLE, EVGroup, and Karl Suss. BPS Technologies has recently introduced an automated de-mount tool for use with perforated carriers. Also, glass carrier disc vendors, such as Logitech (Struers, Inc.) and PlanOptiks, have recently introduced doped borosilicate glass carriers with the thermal coefficient of expansion more closely matched to GaAs. These are being tested as a less expensive alternative to sapphire with possible savings of up to several hundred dollars per carrier.[2, 8, 9]

For post grind wet etch, single wafer and batch tools are available from vendors, such as Semitool and SEZ. Single wafer tools tend to offer a tighter total thickness variation (TTV), while batch tools are much less expensive and have higher throughput.[2, 6, 10] Also, vendors, such as Strasbaugh and Speedfam-IPEC, offer high throughput wafer chemical mechanical polish (CMP) systems that can also be used for back-side GaAs wafer post grind damage removal. With these CMP systems, a TTV of less than 2 µm across a 150 mm diameter wafer can be achieved. However, note the TTV of the carrier plus mounting medium can be as high as 8 µm, which is an issue when the final target thickness of the wafer is 50 µm or less.[2, 8, 9]

High density plasma etch tools based on ICP and dual frequency enable single 150 mm diameter wafer via etch processing with high throughput, even for individual source vias (ISVs), which fit within 30 µm long front-side source pads of power FET devices.[11-13] This allows better heat conduction away from the hot active regions of the device.[14, 15] Vendors offering high density plasma etch tools for via etching include Oxford, STS, Tegal, Trikon, and Unaxis.[11] For high aspect ratio ISVs, bias, long throw, or collimated sputter deposition may be required to ensure conformal seed layer deposition through the vias.[16] Some 150 mm Fabs with ISV capability have gone to a cluster platform with individually configured chambers. The cluster platforms are available from Trikon, Unaxis, and Veeco. For Fabs with less stringent via aspect ratio requirements, an automated batch sputter system from vendors such as Astex, TEL, and Unaxis, can be used for seed layer deposition.[1, 3]

Wafer electroplating systems with pulse capability and carefully engineered solution circulation are being used to deposit a conformal thick gold layer (3 to 8 µm) onto the back-side surface and through the ISVs. Vendors marketing wafer plating systems to GaAs Fabs include EEJA, Reynolds Tech, Semitool, and Technic. For wafers to be thinned to 50 µm or less, a thicker back-side gold layer can improve the mechanical strength of the thinned wafer at the expense of slower throughput at the plating step. If the die are to be attached to packages or carriers for module assembly using a high thermal conductive epoxy, then a solder-stop layer inside the vias is unnecessary. If the die are to be attached using Au-Sn eutectic solder pre-forms, then a solder-stop metal, such as Ti, TiW, Ni, or Cr, that readily oxidizes needs to be deposited inside the vias to prevent solder from "blowing out" the front-side metal pads.[1, 3] The solder-stop layer can be deposited by either sputter deposition or electroplating. A photolithography / wet etch process is typically used to completely clear the solder-stop from the back-side metal plane in order to minimize voiding at this interface during the die attach step. For large via openings at the back-side surface, the thick, positive, liquid photoresist flows into and fills the via during the dispense step. This enables a flood exposure and develop process to be used after back-side dicing streets have been defined saving one contact mask step.[1, 3] During the photoresist bake step, it is possible for some solder-stop metal to diffuse slightly into the thick gold layer along grain boundaries. This small concentration of diffused metal can later oxidize and create voiding problems at the solder die attach step. A quick fix to this problem is to implement a short gold wet etch (either potassium iodide or cyanide based) to lift off the solder stop metal imbedded in the grain boundaries. Finally, the photoresist mask is wet stripped, and then the thinned wafers can be de-mounted from the carriers.[1-3, 6]

Dicing of thinned wafers less than or equal to 100 µm thick may require the use of UV dice tape, especially if the wafers are to be sawn.[4, 17] The structure of UV dice tape is very similar to that of UV BG tape as shown in Figure 1. Vendors recommend that the UV dice tape be exposed within 24 hours after the wafer is mounted on a tape frame in order to ensure that residue from the adhesive binder is not left on the die after pick & place.[17, 18] If this is not followed, then residue can potentially lead to problems if a Au-Sn eutectic solder die attach step is used. Upon UV exposure the adhesive strength of the tape is decreased between one and two orders of magnitude.[19] This enables thin, fragile die to be pick & placed from the dice tape.[4, 19, 20]

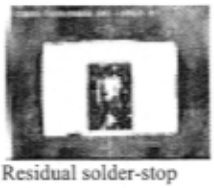
Au-Sn Eutectic Solder Die Attach

Most GaAs device die with back-metal are attached to packages or module carriers using conductive thermoset epoxy. However, for high power devices, a Au-Sn eutectic solder with a melt temperature of 280°C may be needed to satisfy the thermal conduction requirements between the active region of the device and the heat sink. The two main tool platforms for Au-Sn die attach are a pick & place, hot forming gas die bonder and reflow oven.[20-24] With the recent advances made in robotics, vendors, such as Palomar Technologies and MRSI Group, now offer fully automated platforms.[20, 24] For high power devices that need to be die attached using Au-Sn eutectic solder, a smaller die size is desired to achieve a more robust die attach process.[20] A void-free die attach may be required to ensure adequate thermal conduction of heat away from the power amplifier active regions. For the pick & place die bonders, larger size die typically require a higher forming gas flow in order to promote an increased heat transfer rate and reduce voiding between the solder pre-form and die back-metal surface. Also, a programmed scrub breaks down the tin-oxide on the pre-form prior to forming gas flow.

C-SAM (C-mode Scanning Acoustic Microscopy) can be used as a periodic screen test to check for excessive voiding between the die and carrier after die attach.[21-23] It is also useful in optimizing a die attach process. Since the package or module needs to be submerged in DI water, the test can be destructive if it is non-hermetically sealed. C-SAMs of three Au-Sn eutectic solder pre-form die attachments done with a pick & place, gas die bonder are shown in Figure 2. The first die attach was essentially void-free since tiny voids occurred only at the vias, which are lined with solder-stop metal. The second die attach had a few large voids as a result of residual solder-stop metal on the die back-metal surface. This was confirmed by Auger Microanalysis. The third die attach has a large void due to partial wetting of the pre-form. This was traced to a forming gas nozzle

misalignment, contributing to a partial pre-form to reach the eutectic melt temperature.


a. Good die attach


b. Residual solder-stop


c. Gas nozzle mis-aligned

Figure 2: C-SAMs of void-free and void problem Au-Sn solder pre-form die attach. Voids are white.

Depositing Au-Sn directly onto the back-side of the wafer is being explored as an alternative to the use of Au-Sn eutectic pre-forms, stamped to accommodate specific die sizes. The Au and Sn can either be deposited sequentially [25, 26] or jointly[27] to try and achieve the eutectic composition needed for die attach. Also, a Au "sealcoat" layer can be deposited to prevent the Sn from oxidizing before or during the die attach.[25, 26] This should lessen the demands on the scrub and hot forming gas flow steps to reduce surface oxides. The eutectic Au-Sn pre-form thickness is typically in the range of 25 µm, necessitating the use of a solder-stop layer inside the vias. The deposited Au-Sn layer or total composite layer thickness can be tailored to obviate the need of a solder-stop layer. With the recent advances made in wafer electroplating equipment, depositing Au-Sn directly onto the wafer back-side may shortly move from the R&D phase into manufacturing.

Temporary Wafer / Carrier Mounting

Wafers that require back-side vias and metal need to be mounted on a carrier using a mounting adhesive. These adhesives are available in a variety of forms such as sticks, films, and liquids.[1-3, 6-9, 28] Although each adhesive may offer its own benefit in mounting, the most robust system will be that one which maintains its integrity during each back-side step. At least one vendor, General Chemical Corporation (GCC), is promoting the benefits and cost savings to Fabs through the use of an entire materials support program for back-side processing.[29]

Most adhesives used in wafer mounting exhibit thermoplastic character. Heat is commonly used to achieve uniform metrology and adhesion. Adhesives may be heated to aid flow, topology penetration, and wetting. Taken together, these will produce a smoother surface in preparation for mounting.[28]

During wafer to carrier mounting, maintaining substrate planarity and uniformity is believed to be a key parameter in successful thinning.[30] Good surface planarity, usually measured as a low TTV, is believed to reduce both internal stress and wafer bow during grinding.[28, 30-32] Liquid spin-on forms of adhesives offer easy control of TTV.[30] However, variations in TTV for certain spin-on adhesives exist. Pentalyn™H [33], a customer's prepared product, and GenTak™ [34], a ready-to-use dual polymer system, are shown in Figure 3 to have a TTV of nearly 10 and 0.03%, respectively, for a 10um target thickness.[28]

GenTak™ may be available in a variety of viscosities offering flexibility in the application to different substrates. Different viscosities allow a variety of ways to achieve planarization of different topographies and to coat-up a range of thicknesses as shown in Figure 4.

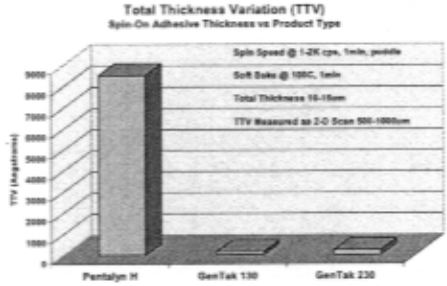


Figure 3: TTV of cured spin-on adhesives.

An ideal spin-on adhesive should have wafer edge bead and cured residue on coating equipment easily removed with commodity solvents, such as PGMEA or acetone, as well as be compatible with the existing resist waste stream.[35] Certain spin-on adhesives, such as GenTak™, offer full compatibility with the use of common positive resists.[28]

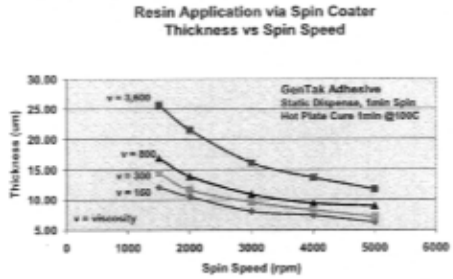


Figure 4: GenTak™ liquid adhesive application spin curves.

Once the adhesive is applied and cured, mounting proceeds through a thermo-mechanical process. Typically, temperature, pressure, and time are controlled. However, these parameters and the extent to which they are controlled will depend upon the adhesive, coating method, mounting tool, and whether or not perforations exist in the carrier. In all cases bonding and flow temperatures in excess of subsequent back-side processing temperatures are warranted in order to reduce out-gassing and prevent undesired adhesive flow.

Substrate / Adhesive-Safe Via Cleaning

Dry etching of vias using ICP, high density dual frequency, or RIE requires sidewall passivation in order to achieve an anisotropic profile. During the plasma process, small amounts of organic residue from the eroded photoresist mask is redeposited upon the via sidewalls. This sidewall residue is usually very thin on the order of angstroms. The sidewall residue composition is commonly an amorphous mix of plasma substrate ions, resist by-products, and plasma reactants, which form unknown organometallics.[36] This passivation layer must be removed prior to back-side metal deposition.

Via cleaning is commonly done through chemical stripping with solutions having high levels of amines.[37] These chemistries are time intensive and require a balance between cleaning performance and unwanted substrate etching or adhesive removal. An alternative approach exists in using adhesive and substrate safe materials with robust agitation utilizing ultrasonics. The combination of specialty chemistries, such as GCC's GenSolve™ 600 series,[38] and using high frequency ultrasonics at low generator power are showing

Summary

The two branches of back-side wafer process flows for a typical GaAs Fab were presented. New equipment and methods that have recently become available to handle some of the historically troublesome steps were discussed. Emphasis was placed on the Au-Sn eutectic die attach and the temporary wafer / carrier mounting steps. Through the use of robust applications and high performance materials, backside processing of GaAs wafers can be optimized to reach high volume throughput and yield requirements.

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