DaeBond 3D™
A High Throughput Thin Wafer Support Technology for 3DIC

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New Wafer Process for 3DIC

Technology Abstract

- DaeBond 3D™ is a disruptive technology
- Device wafers are planarized with an inert coating, bonded to a porous coated carrier, and processed.
- De-bonding occurs by capillary-driven penetration through the porous layer.
- Carrier release is <15min while the device wafer is supported onto a taped film frame.
- The batch driven process is conducted in a simple wet bench where cost and throughput is defined by cassette size

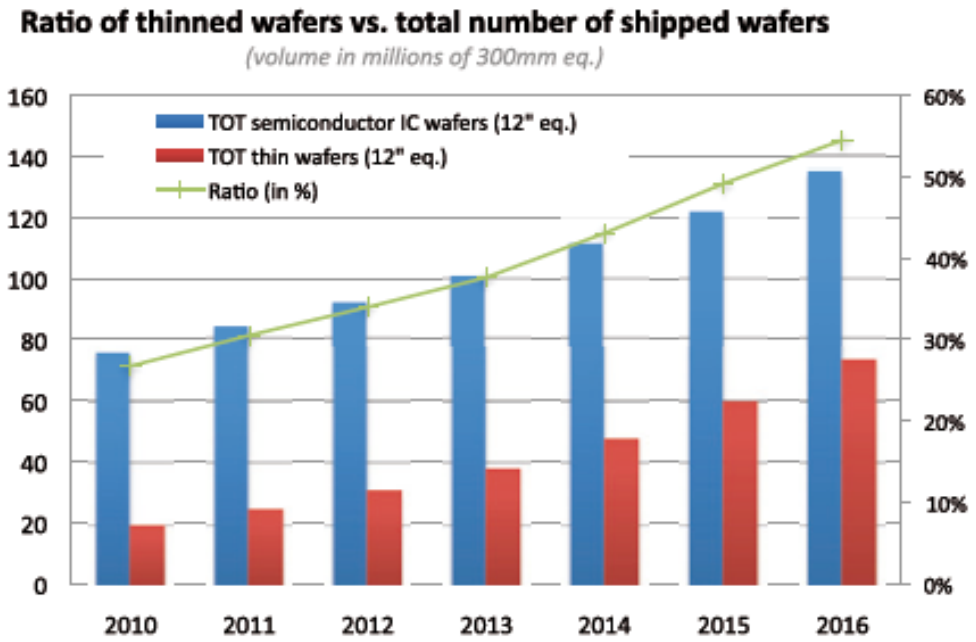
Agenda

1. Background
2. 3DIC Technology Status
3. DaeBond 3D™
4. Summary

1. Background

Trending to Thin Substrates

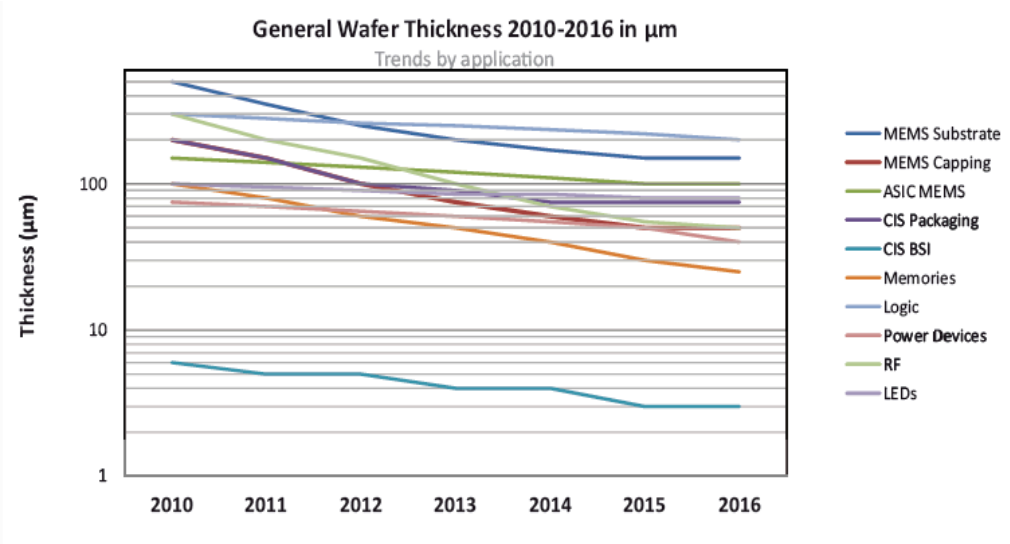
- 25% thinned
- Soon to be 50%



Courtesy: Yole Development

Thinning below 100um

- Most are <100um
- Current target <50um
- ~5yrs <30um



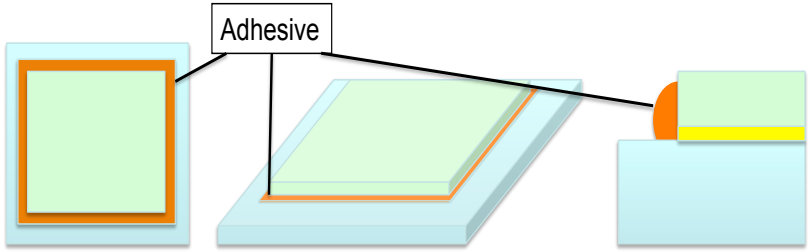
Courtesy: Yole Development

Daetec's Model

- Historically, Daetec is an open innovation technology development firm
- Completed >25 tech transfers, ~6mos ea.
- Focus on thin substrate handling, cleaning
- Markets include semiconductor & display
- This year, product sales have begun in our division: www.waterwashtech.com

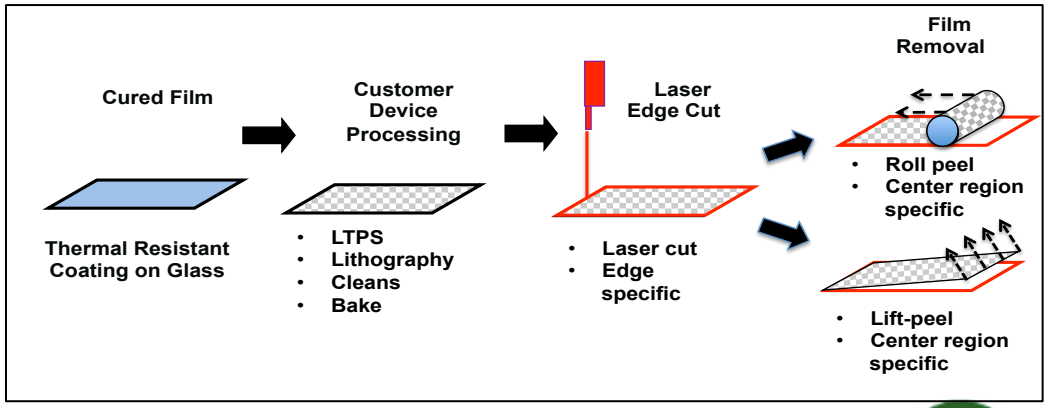
Daetec's Enabling Technologies Processing Thin Display Substrates

Thin Glass



SAMSUNG
SHARP
AUO
LG

OLED Films



DAETEC

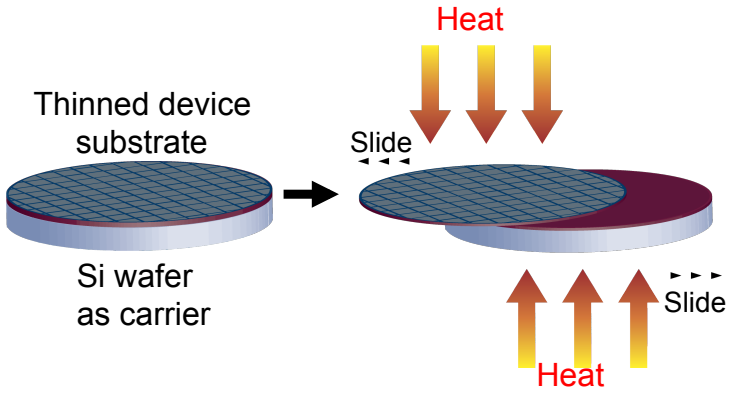
iMAPS

Daetec's Enabling Technologies
Processing Semiconductor Substrates

Materials

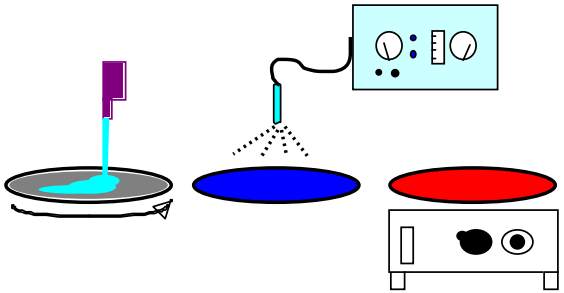
brewer science

HT10.10 Adhesive



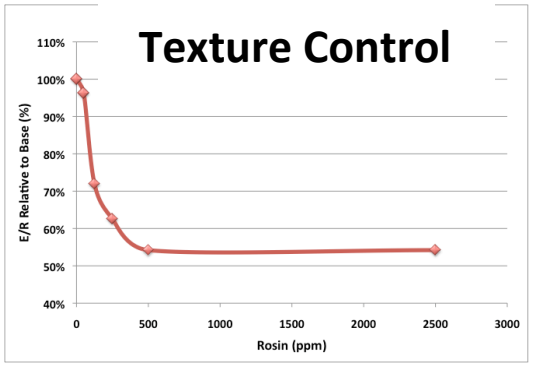
Equipment

SÜSS MicroTec

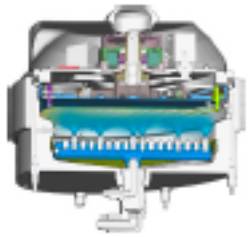


Processes

SSEC



Bulk Si Thinning
Chem Etch

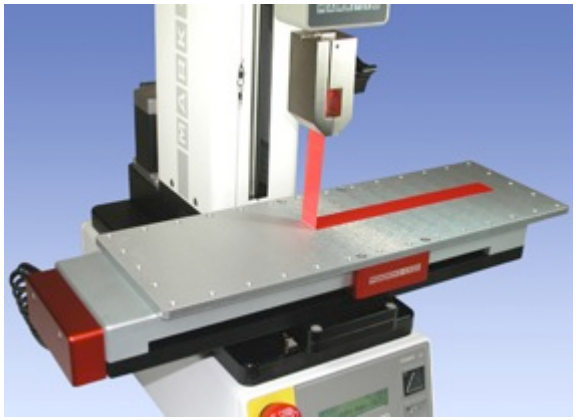


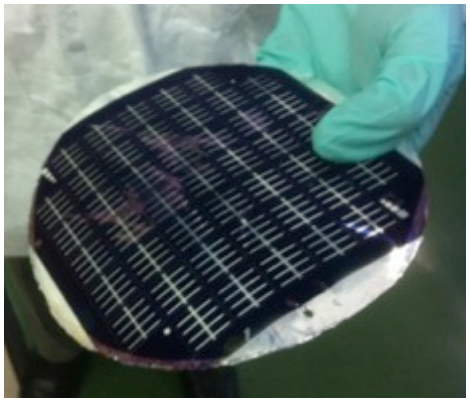
Spray Acid

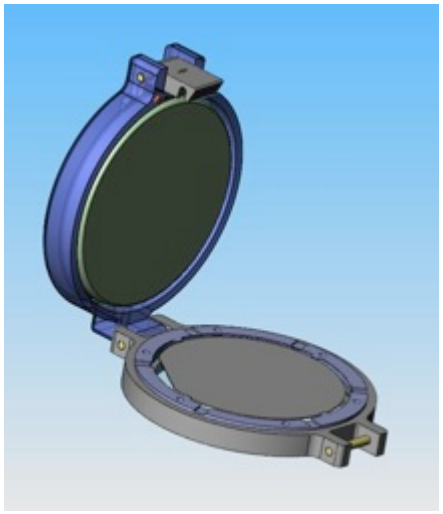
SEMITOOL

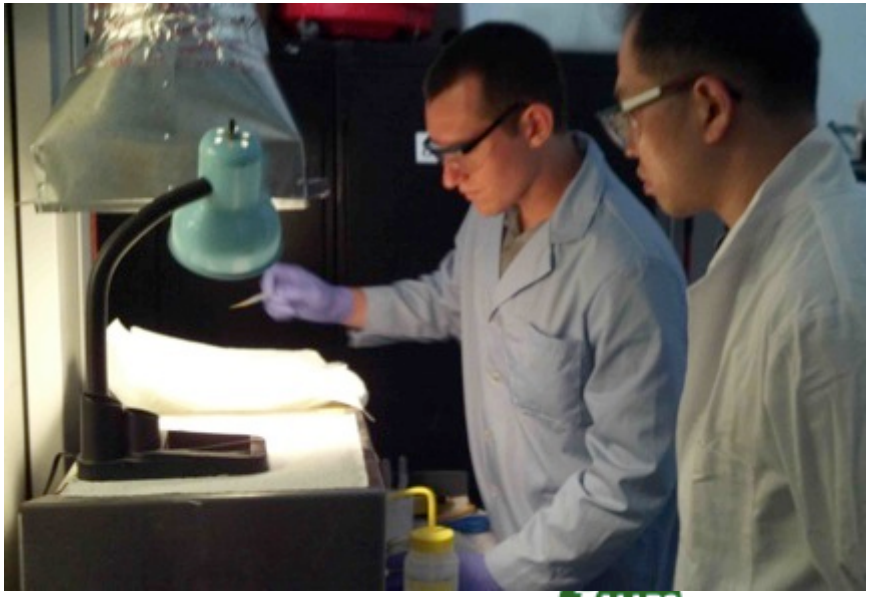
DAETEC

Process Development



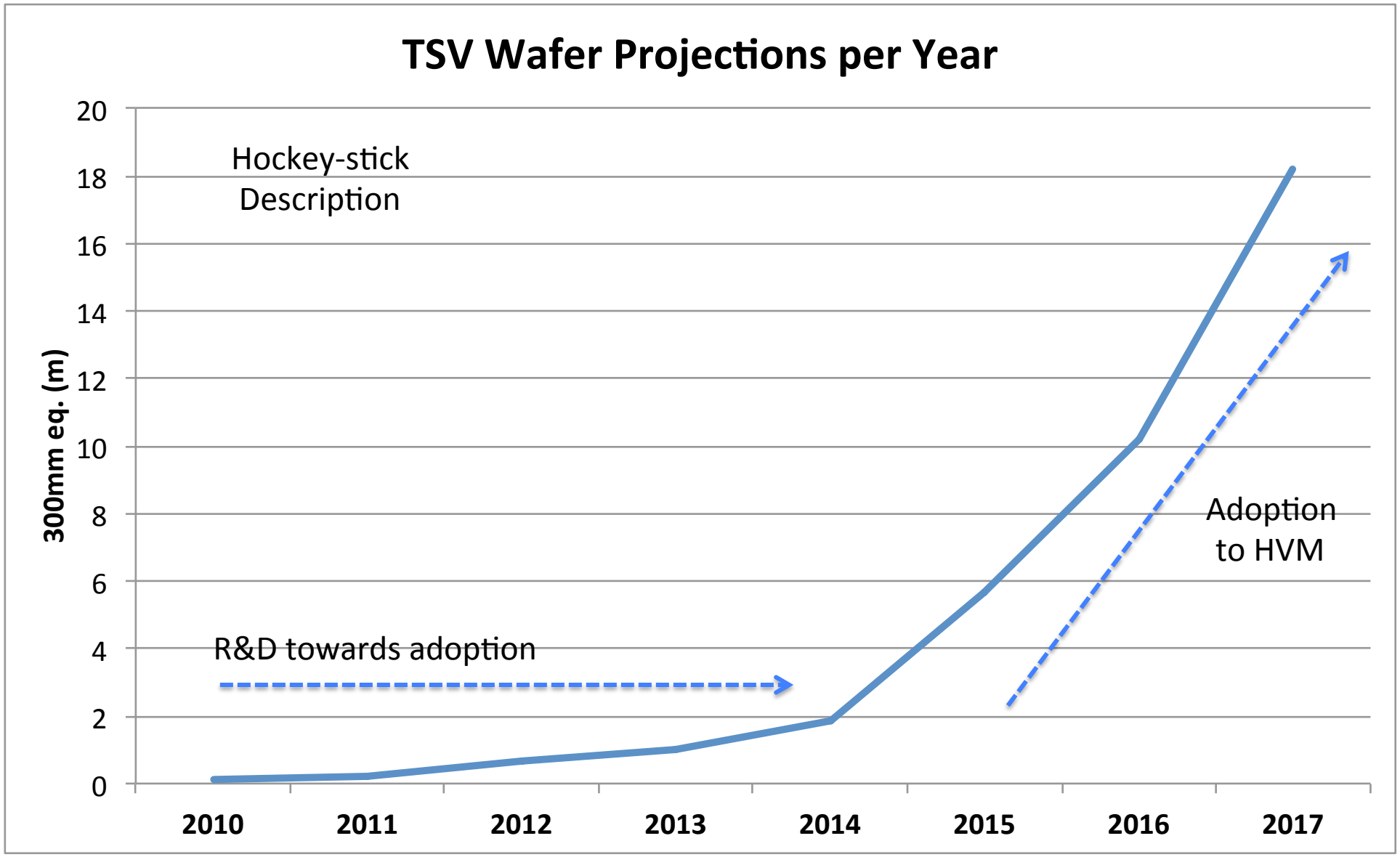






2. 3DIC Technology Status

- Semicon-West 2013 panel of experts:
  - 3DIC is one of the top industry challenges
  - Devices manufactured at ≤30nm node require flip-chip, bump, and creative connectivity
  - Tool costs are high and of low throughput
    - TSV etch, plating, bond/de-bonders, $1.5-8m each
    - Target 20wph
  - 450mm scaling is unknown



Source: Gartner 2013

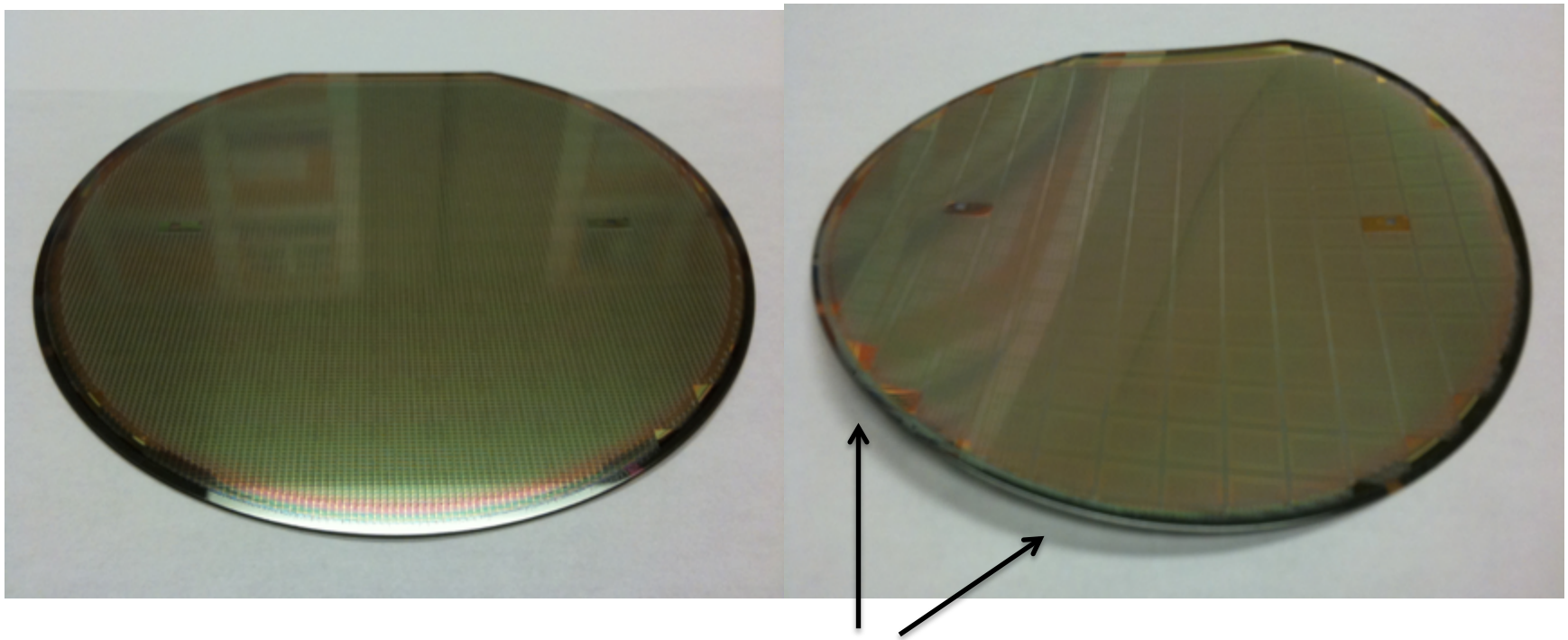
3DIC Enabled by Temporary Thin Wafer Support

- Adhesive: Mount device wafer to carrier
- Carrier: Silicon or glass, sapphire
- Temporary: Meet mechanical and chem. resistance, seal front side, remove
- Backside processing: Insert connections (lithography, etch, metallize)
- Debond: simple, low cost, substrate safe
- Cleaning: complete, no residue

Thin Wafers Require Support

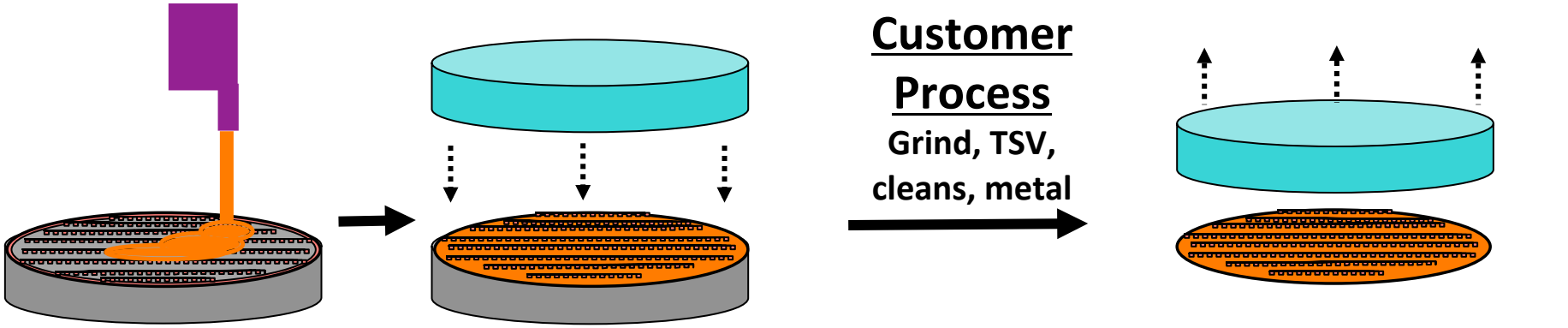
Full thickness ~ 700um

Thinned ~ 100um



Stress introduction causes wafer bow

Temporary Bonding Process



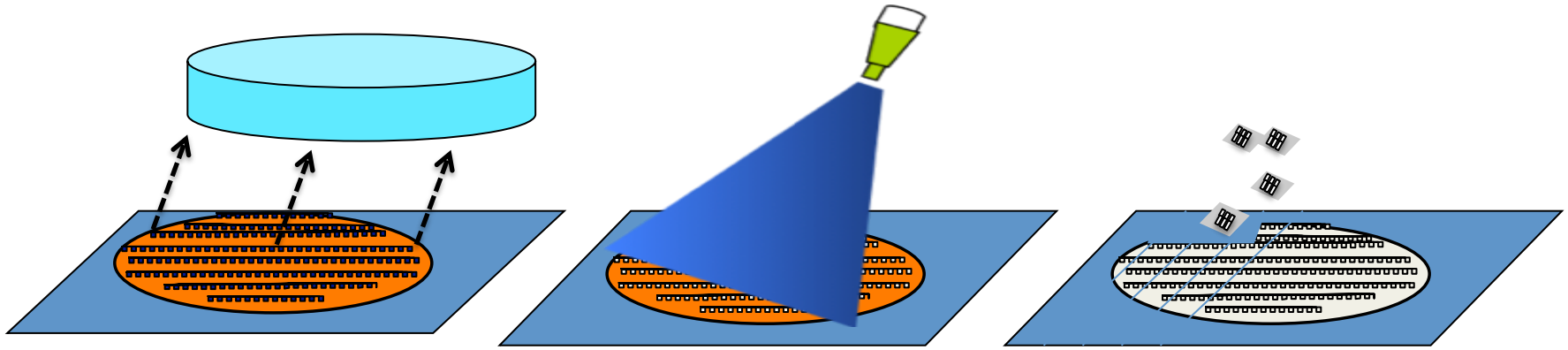
Bond **De-Bond**

Two ACTIVE steps
"Bonding" is similar between all
Differences occur during "De-bond".

Existing Technologies

Supplier	Product	Chemistry	Thermo-reaction	De-bond	Process Type
BSI	WaferBond™	Rubber	Plastic	Chem. diffusion w/perf. carriers, thermal slide, ZoneBond	Single & batch (perf. carrier)
3M	LTHC™ & LC-series	Acrylic	Set	Laser assisted debond + peel	Single
DuPont	HD™ 3000-series	Polyimide	Plastic	Chem. diffusion w/perf. carriers, laser ablation	Single
TMAT	Release layer + adhesive	Silicone	Set	Pull-apart	Single
Dow-Corning	WL-series adhesive + release layer	Silicone	Set	Pull-apart	Single
TOK	Zero Newton	Urethane	Plastic	Chem. diffusion w/perf. carriers	Batch (perf. carrier)
DOW	Cyclotene	BCB	Set	Chem. diffusion w/perf. carriers	Batch (perf. carrier)

Roadmap to Dicing



Film Attachment Carrier Demount

Wafer Cleans Safe for Tape

Dicing

cleans compatible to tape or vice-versa

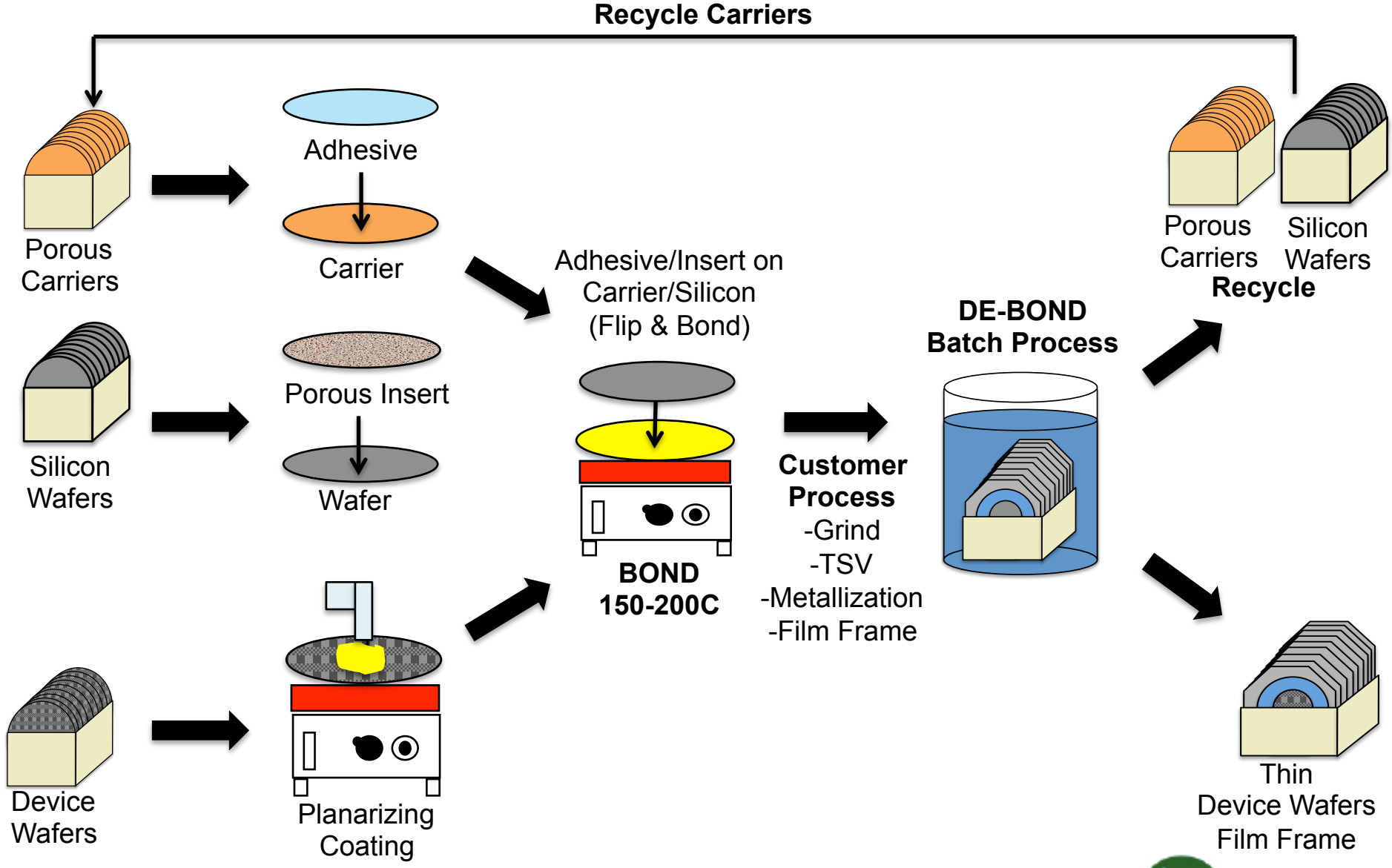
Barriers to 3DIC

- Single wafer process, perforated carrier
- Low yield – physical stress to device wafer
- Low throughput – have 8-12 wph, want 20
- Unsupported thin substrate
- Cleans not compatible with tape film frame
- High tool cost
- Carrier not recyclable
- Not scalable

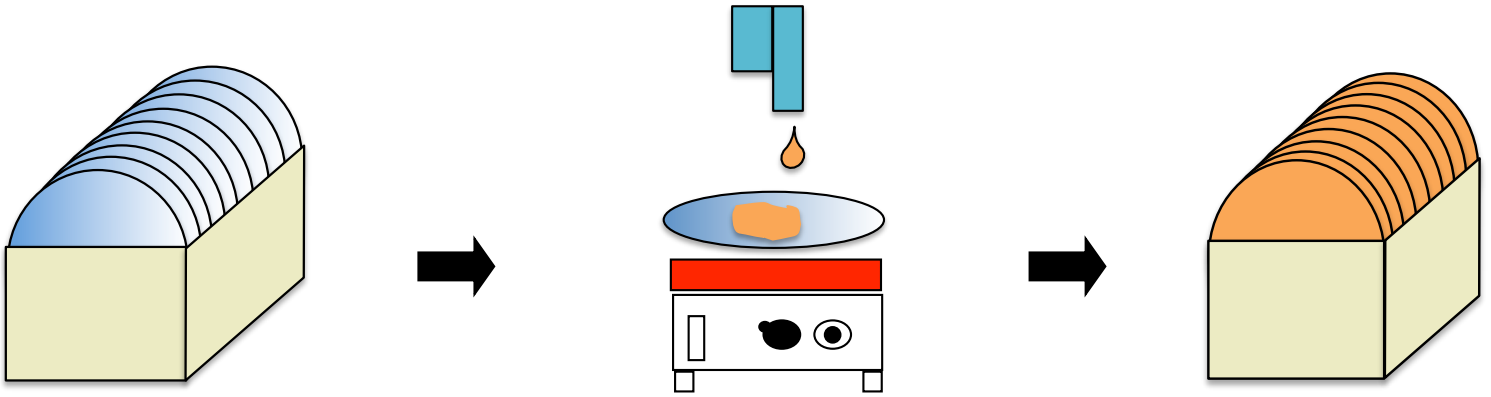
3. DaeBond 3D™

Benefits	Explanation
High Yield	Planarized layer – protects features, DIW soluble Continued support – film frame Passive de-bond – no mechanical slide, peel, pull, or burning
Adhesive	Chemical & thermal resistant, soluble in tape-safe chemistry
Simple & low-cost tool	De-bonding conducted within common wet-bench
High Throughput	100wph baseline
Taped film frame	Compatible with tape-safe de-bond chemistry, DIW cleans
Porous carrier recycle	No cleans required, 10 cycles before re-apply
Scalable	Penetration/saturation is non-linear relative to substrate size; de-bond time increases by a minor factor
Green process	Tape-safe de-bond, DIW cleans

Porous Coat & Insert



Porous Coating on Carrier Wafers

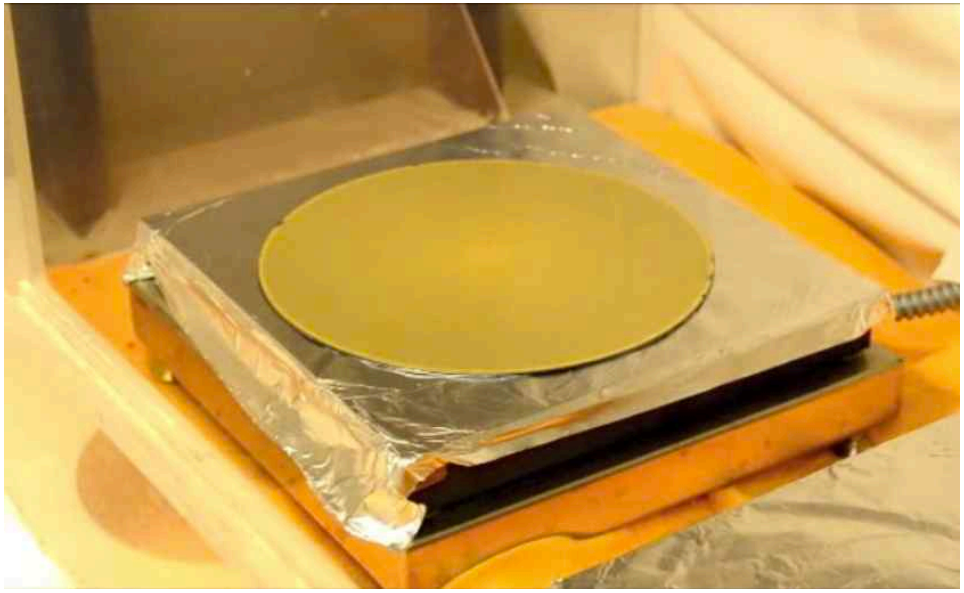


Carrier Wafers

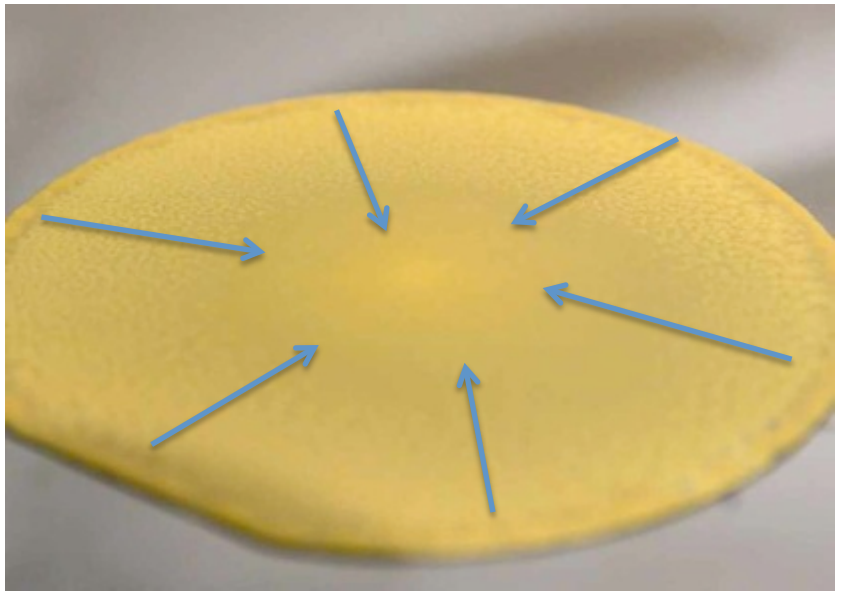
Porous Coating
& Cure

Carrier Wafers
w/ Porous Coat

Formation of Porous Carrier



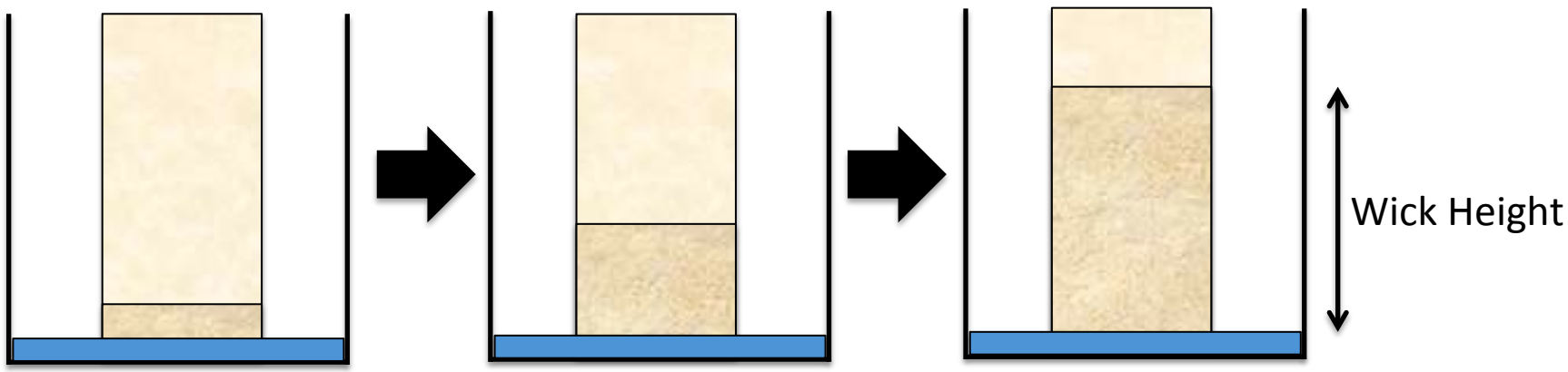
Apply Coating to Si Wafer



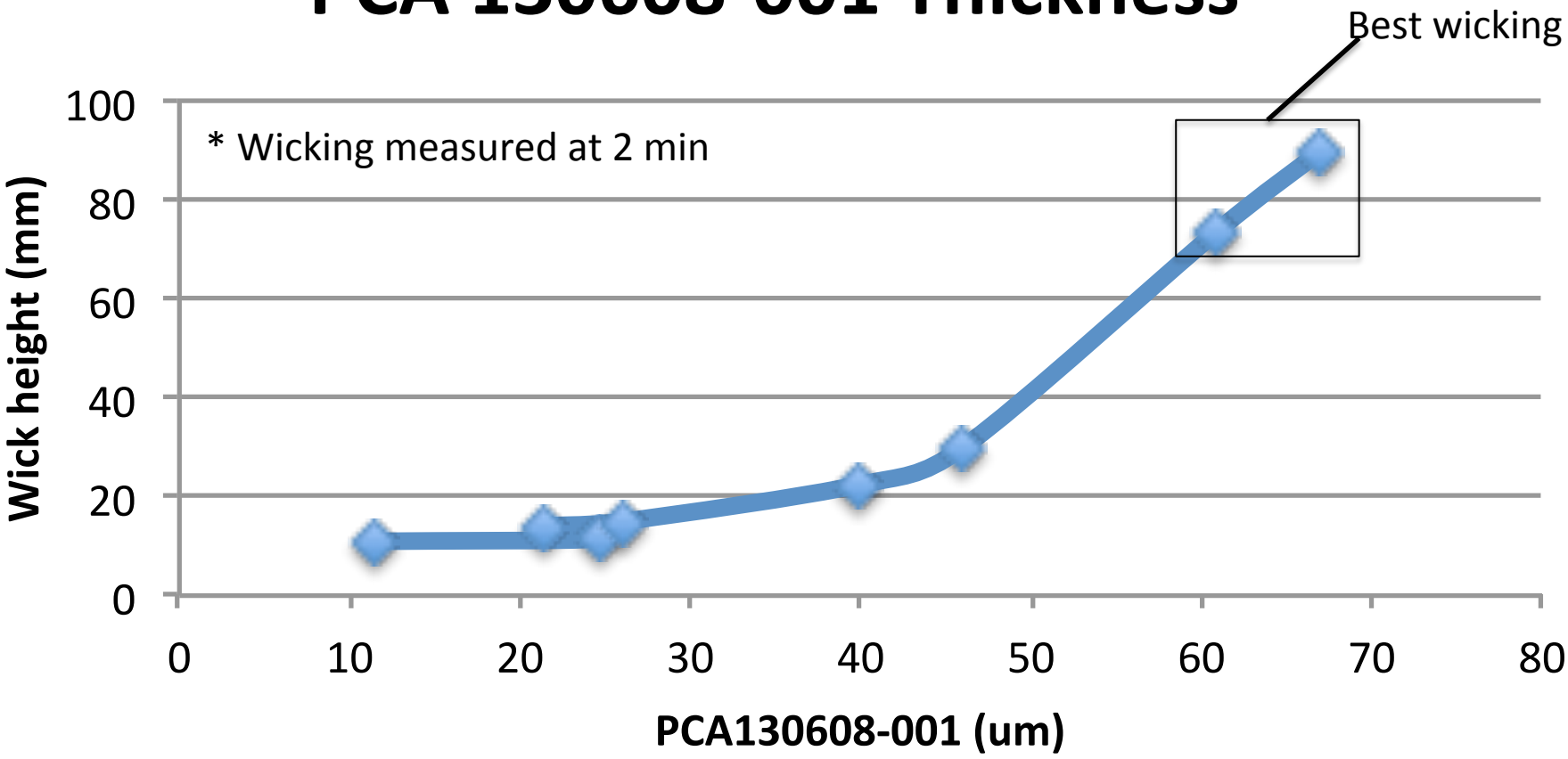
Porosity production during cure

Porosity Method (Wick)

- Daetec's method
- Application related to porosity



Wick Height vs PCA 130608-001 Thickness



Planarization Coating

- Planarizing over topography
- Achieves >100um thick coatings
- Rigid to protect during grind & handling
- Inert, non-crosslinking, no reaction with metals, organic materials
- Thermal resistance >300C
- DIW soluble, removed in tank #2

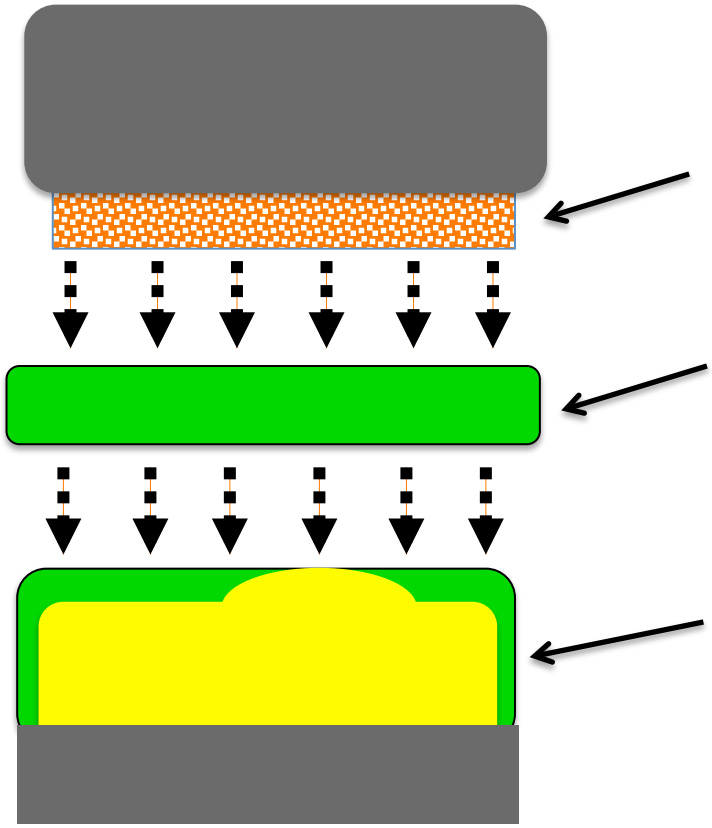
Planarization Coating

Wafer with Topography (planarize >100um)

Planarization Coating

Planarized Surface

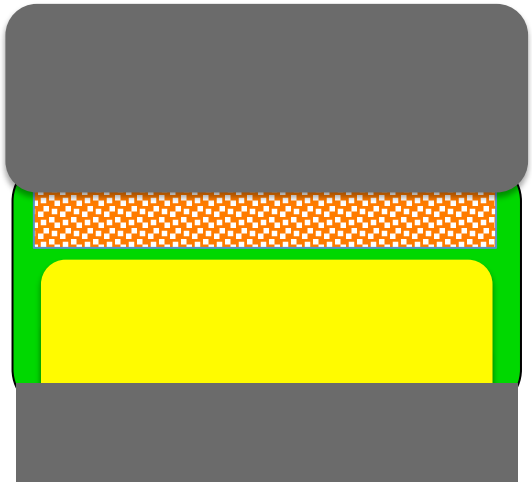
Porous Carrier & Sealed System



Porous Coating

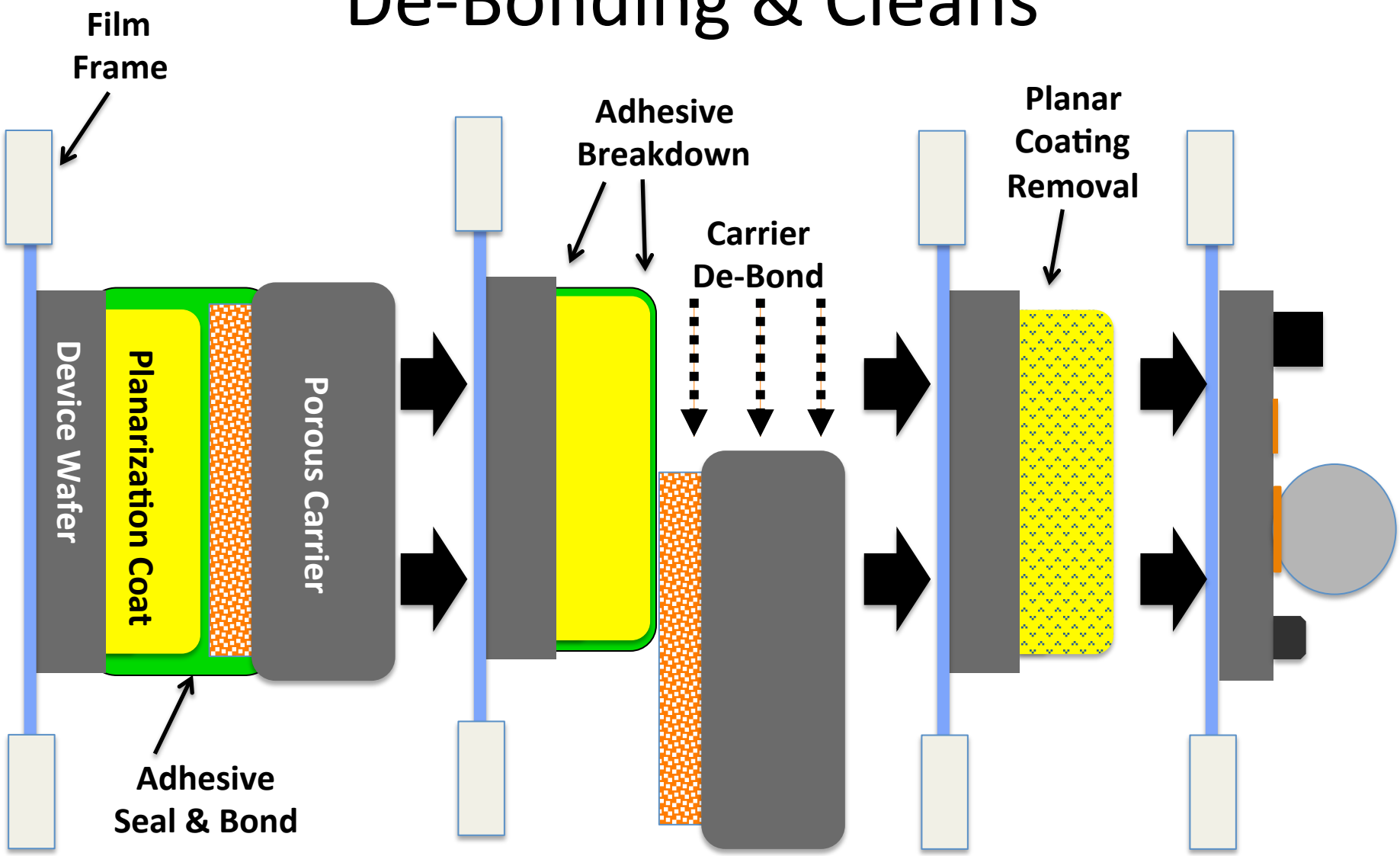
Adhesive

Planarized Coating + Adhesive Edge Seal



Bonded & Sealed System

De-Bonding & Cleans



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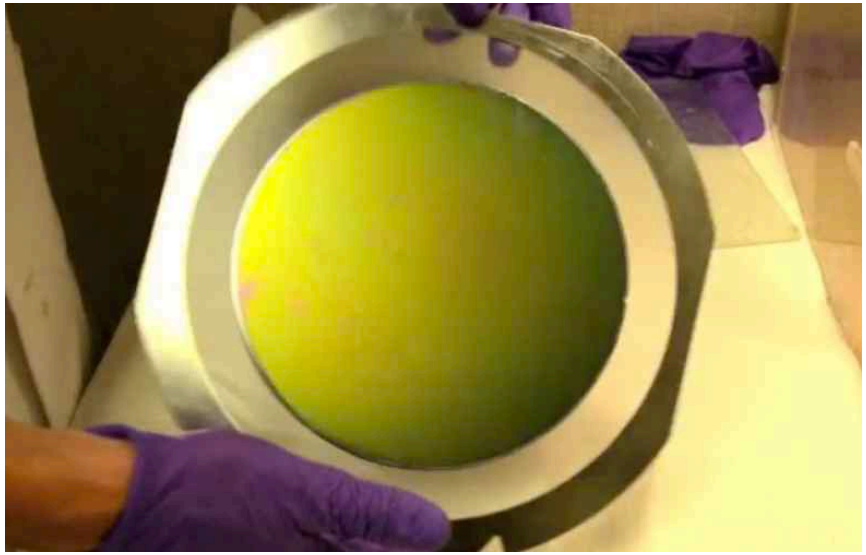
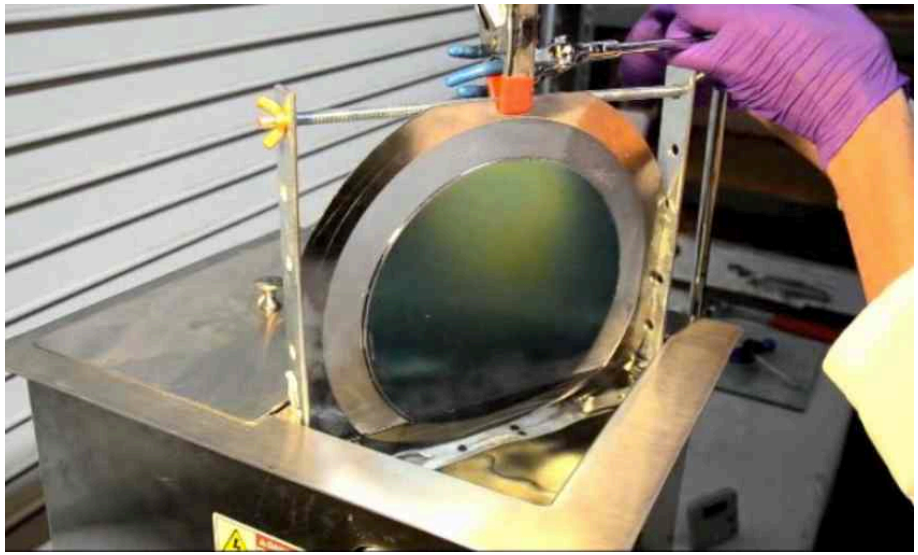
Affix to Film Frame for Debond

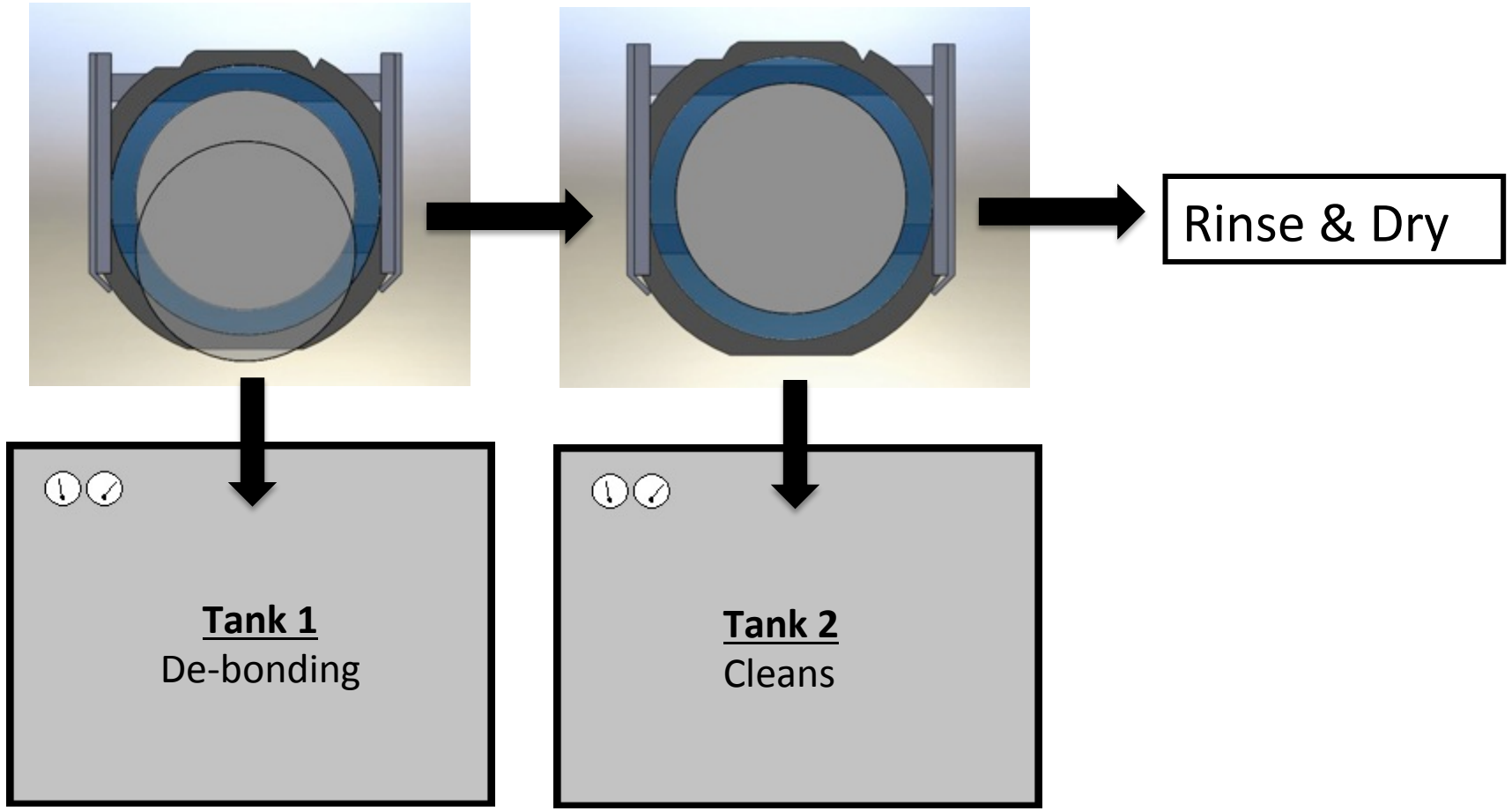


Film frame attach
Bonded stack

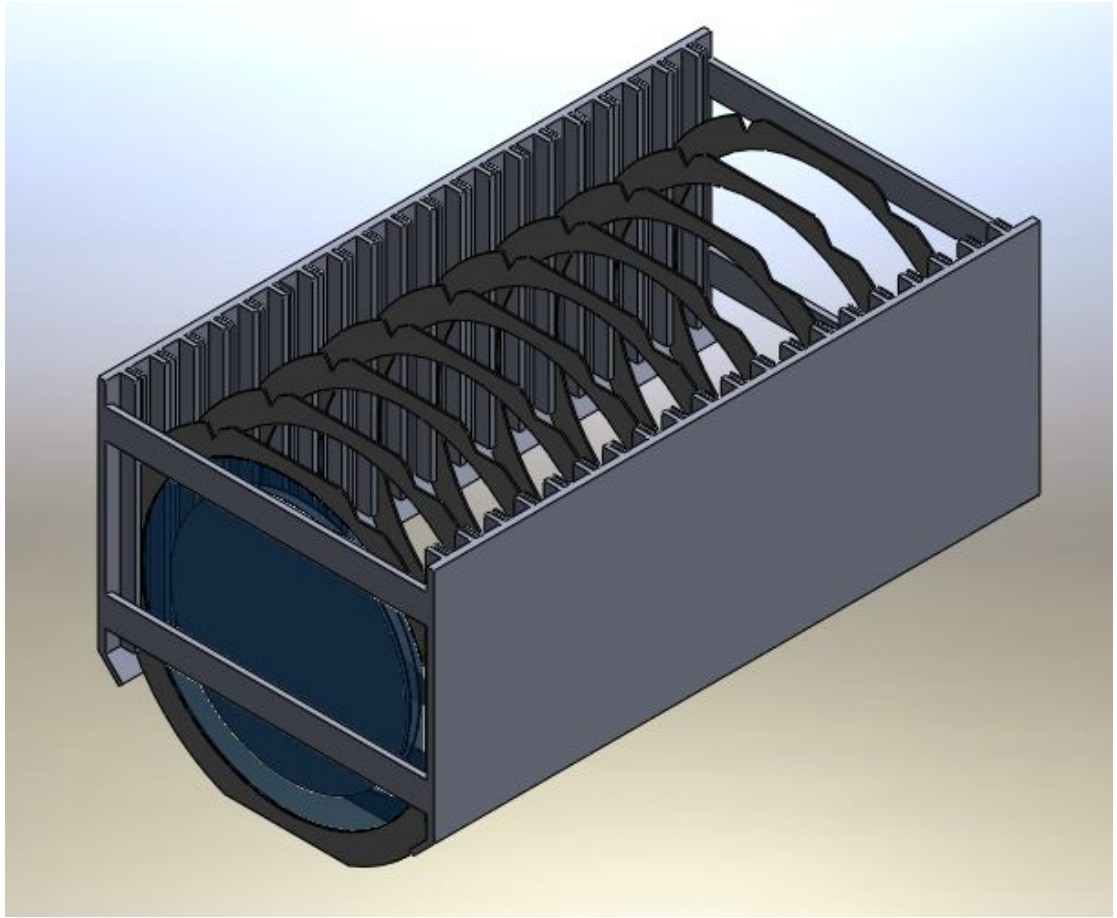


Daetec single wafer fixture

Debond Process

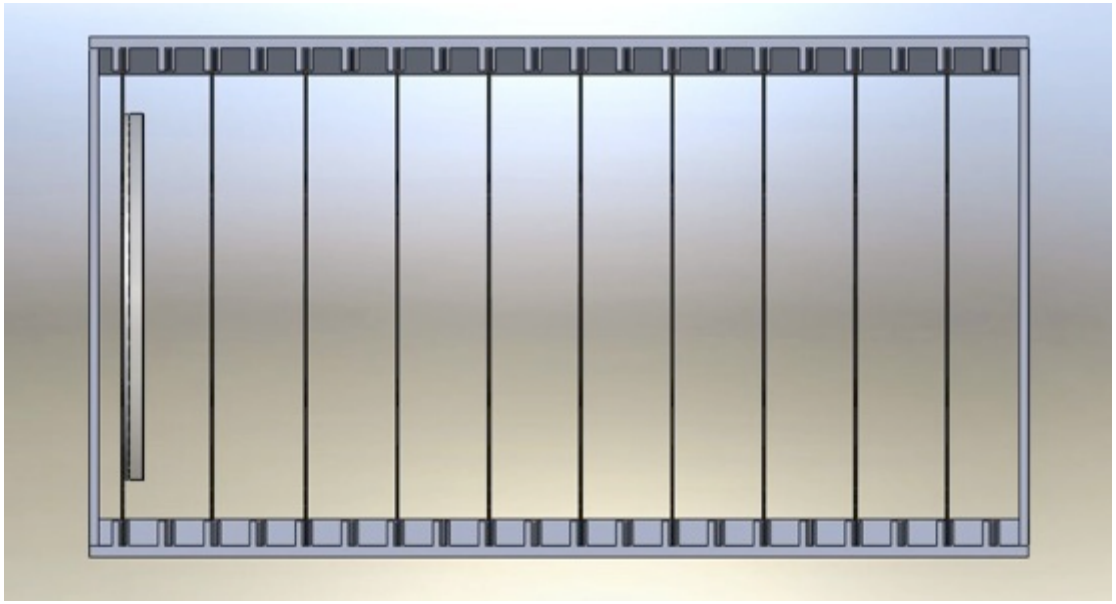


Debond Fixture for Multiple Wafers



- Open-body design to allow chemistry circulation
- Bonded film frame rings are vertically loaded into slots

Fixture Features



- **Full scale** processing: 20-25 wafers, <15 min

  -OR-

  80 – 100 wafers,1 hr

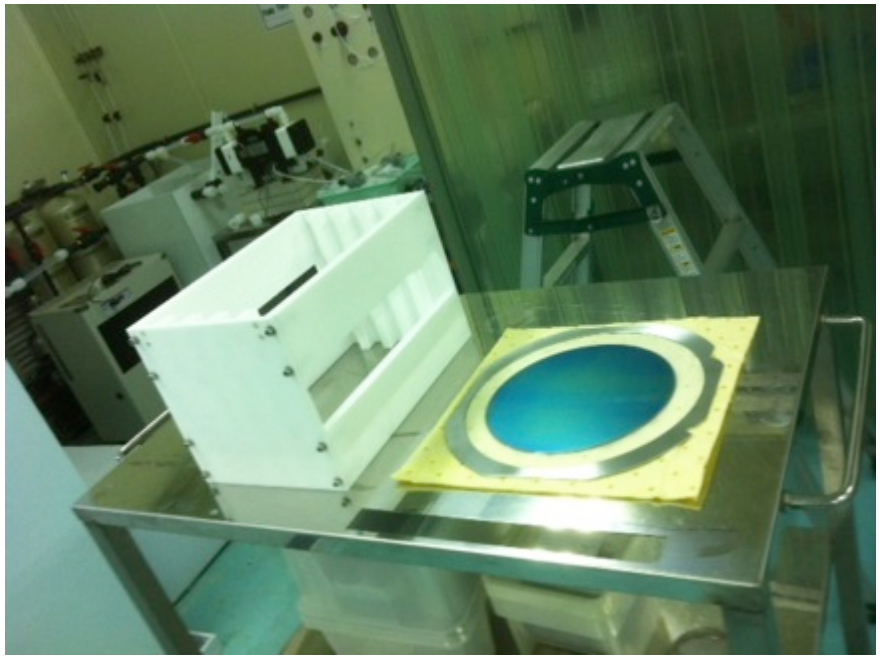
- **Prototype** processing: 4 wafers, <15min

Demo in Daetec's Tool

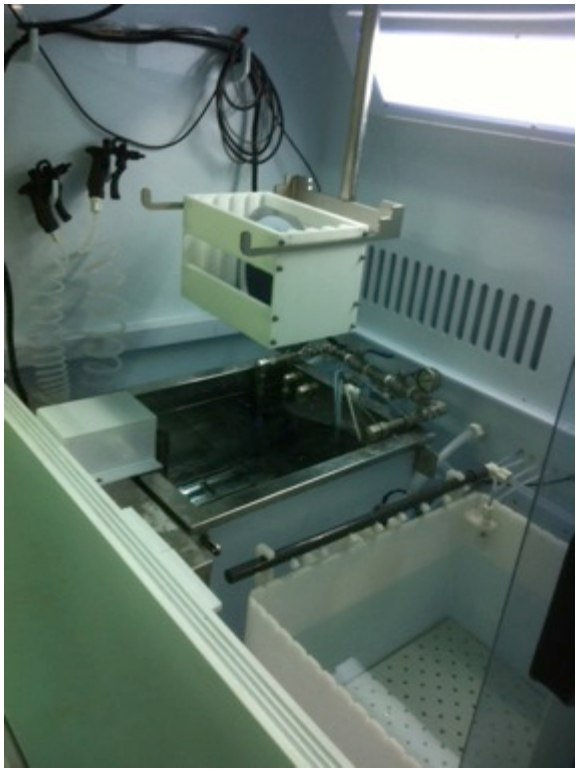
Wafer capability:

- 6”
- 8”
- 12”

Tool Demonstration

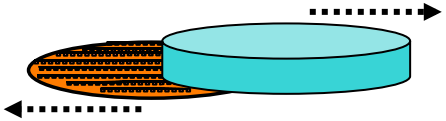


Fixture w/film frame



Operation in wet bench tool

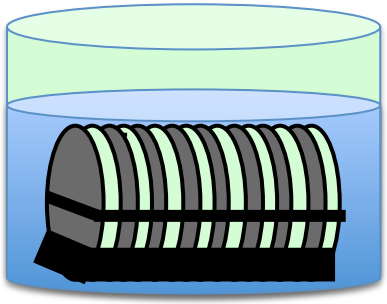
Process – Debond/Cleans



Slide/Debond + Clean

Max 20 wph

SW Debond & Cleans



Batch Demount & Cleans

Min 100 wph

Batch Debond & Cleans (Wet Bench)

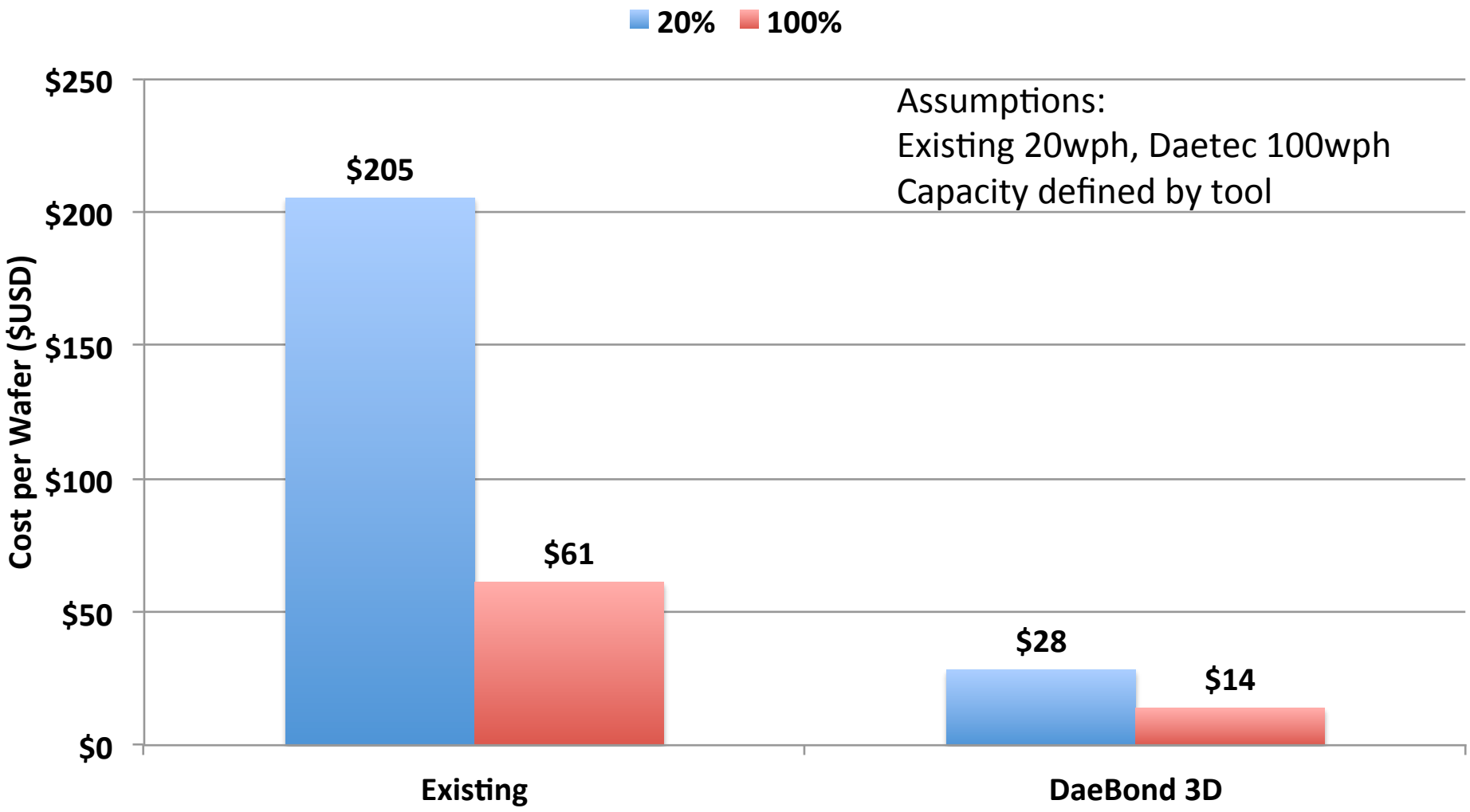
Cost Comparision (for COO)

Parameter	Existing	DaeBond 3D™
Adhesive	Thermoplastic - rubber	Thermoset - blend
Carrier	Silicon	Porous coat on silicon
Materials	Adhes. + solvent cleans	Adhes. + porous coat + cleans
Materials cost per wafer ($USD, <1m/>10m)	$25	$25/$10
Coating Application	Spin	Spin
Thermal Resistance (C)	200-250	>250
De-bond Method	Thermal slide, peel	Porous saturation
De-bond tool type	Single Wafer; slide or peel	Batch; wet bench
Tool cost ($USD m)	1.5	0.75
Throughput (wph, per tool)	20 (target)	100 (minimum)
Cleans Chemistry	Solvent	Aqueous (5% in DIW)

Materials Cost Projection

- Materials include cost on porous carrier and device wafer adhesive
- Estimates based upon 2 volume levels:
  - <1m wpy: ~$25/wafer ($28 w/tool)
  - >1m wpy: ~$10/wafer ($14 w/tool)

Cost per Wafer Existing vs DaeBond 3D™ & Capacity



COO by SEMI E35

- Ratio of technologies
- Cancel out several variables

#	Definition	COO_2 vs. COO_1	Explanation
F$	Fixed Costs	$F\$_1$ = \$1.5m = 5 X $R\$_1$ (yr1) $F\$_2$ = \$0.75m = 2.5 X $R\$_2$ (yr1)	Tool represented as materials cost
R$	Recurring Costs	$R\$_2 = R\$_1$ = \$300K/yr	Materials costs same; 12,000 wpy @ \$25/w
Y$	Yield Cost (scrap)	$Y\$_2 = Y\$_1 = 0$	Assume no loss
L	Equipment Life	$L_2 = L_1$	Same life
T	Throughput	$T_2 = 5 \text{ X } T_1$	batch vs SW = 5 X T_1
Y	Composite Yield	$Y_2 = Y_1$	Same yield
U	Utilization	$U_2 = U_1$	Same maintenance

$$COO = \frac{F\$+R\$+Y\$}{L \times T \times Y \times U}$$

$$\frac{COO_2}{COO_1} = \frac{\text{DaeBond 3D}}{\text{Existing Technology}}$$

$$\frac{COO_2}{COO_1} = \frac{F\$_2 \times T_1}{F\$_1 \times T_2} = \frac{F\$_2}{F\$_1 \times 5}$$

$$\frac{COO_2}{COO_1} = 10\%$$

COO_2/COO_1 Comparison Results

Comparison of COO Technologies	Tool costs 1) $1.5m 2) $0.75m	Tool costs 1) $3m 2) $0.5m
COO_2/COO_1	~10%	~3%

4. Summary

- DaeBond 3D is a disruptive tech for 3DIC
- Technology based upon a porous coating
- Porosity allows passive wafer de-bonding
- De-bonding occurs on film-frame tape
- Process finishes in a film-frame cassette
- Throughput is defined by cassette size and flow, minimum 100wph

Contact for More Information

- DAETEC provides development, consulting, and technical training/support to solve manufacturing problems and introduce new options of doing business.
- Diversified Applications Engineering Technologies (DAETEC)

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