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Through-Substrate Via Etching and Cleaning for High Volume Production Demands

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ABSTRACT

By the use of multi-level plasma etch experimental designs, an alternative method for post-etch photoresist removal, and development of an automated post-etch veil removal sequence; a reproducible method for through-substrate via processing was integrated into high-volume GaAs manufacturing. For the plasma etch portion, optical microscopy and scanning electron microscopy (SEM) were used to determine defect density and via dimensions. Analysis for post-etch veil removal was accomplished using optical microscopy, SEM, and Auger electron spectroscopy (AES). Through a series of evaluations, a chemistry from General Chemical Corporation was determined to be effective at simultaneously removing both the photo resist mask and the etch residues. The final process developed resulted in a through substrate via with approximately an 80 degree, single-sloped sidewall profile that was clean from post-etch veil materials.

INTRODUCTION

Backside gallium arsenide (GaAs) through substrate via processing is a highly mechanical, non-automated process that requires extensive operator intervention.[1] Manufacturers are constantly striving to make this process more manufacturable, robust and cost effective. Through substrate via manufacturing involves wafer mounting to a support substrate (Fig. 1), mechanical and chemical wafer thinning, photolithography, plasma etch, photoresist removal, post-etch residue removal, metallization, and finally, wafer de-mounting from its support substrate. Although each of these is a discrete process, they do interact with one another. Taken together, the production of successful vias requires considerations of material and conditions of the entire backside process.

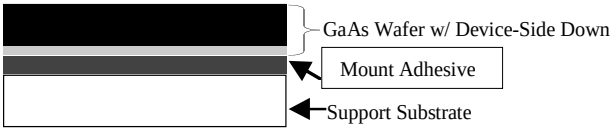

Figure 1 Diagram of a Mounted Wafer

The formation of through-substrate vias on GaAs by plasma etching has been around for some time,[2] but has recently been re-evaluated to decrease grass formation, and decrease post-etch residue (veils). [3, 4, 5] Grass formation and veils create undesirable defects that could affect electrical conductivity and reliability. The intent of this work was to improve via profile while decreasing the possibility of these defects. The desired via profile was a slightly sloped wall extending to via bottom with no sharp edges or undercutting (Fig. 2-left).

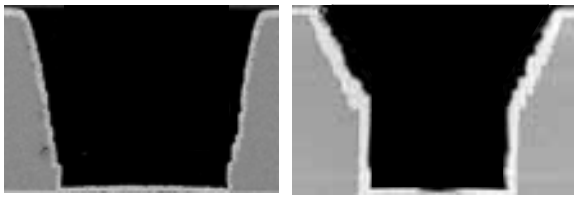

Figure 2 Fully-sloped via profile (left), Champagne-glass shaped profile

Initial via shape resembled a champagne-glass, where the vias have a sloped upper region and a vertical lower region (Fig. 2-right). For several reasons, the fully-sloped via design is beneficial including the production of consistent via dimensions with a large base to maintain a low-inductance connection, consistent sidewall profiles for uniform metal step-coverage and electrical continuity, and minimum top via dimensions to allow a robust layout for current designs and future size reductions.

After the etch process was established, an appropriate veil clean needed to be developed. It was essential for the clean process to be robust and handle any natural etch process variations. With the knowledge gained from AES of the post-etch residues, an attempt was made to determine which chemistry would provide clean vias. Adding to the challenge, process temperatures must be stringently controlled below the softening point of the thermoplastic mount adhesive. Finally, chemical interactions with the adhesive must be carefully considered.

ETCH MODIFICATIONS

Etch experiments were run on 150 mm (100) GaAs wafers mounted on carrier substrates using a thermoplastic material. The wafers were thinned to a target thickness of 90 μm. Photoresist was patterned with 80 μm diameter vias and a gold etch stop was coated on the front side of the wafers. The same mask plate was used for all experiments.

Additionally, for screening of via profiles, SEM was used at a tilt angle of 30 degrees for top-down measurements at the center and edge of wafers. Both top and bottom via diameters, and length of vertical portion of the via sidewall were then measured. Finally, wafers that were screened by top-down SEM work were cross-sectioned and vertical to sloped ratios were determined.

An inductively coupled plasma (ICP) via etch process that uses a BCl_3/Cl_2 gas chemistry was utilized for experimentation. The etcher has an electrostatic chuck (ESC) and helium backside cooling. Under plasma conditions, it is crucial to maintain temperatures below 100°C at the wafer surface to prevent carbonization of photoresist. Maintaining wafer temperature is also desirable to prevent decomposition of the thermoplastic mount material. Final process temperatures measured 43°C at wafer center and 48°C at edge.

The first step in the etch process is an *in situ* descum step to remove any potential photoresist scumming. The descum is followed by a breakthrough step using a BCl_3/Cl_2 chemistry. For the main etch step, a mixture of BCl_3/Cl_2 chemistries is used. Descum and breakthrough steps are often used to minimize pillar or grass formation due to contamination, residual photoresist, or non-uniformities in the substrate.[2, 3]

An initial screening experiment was run to determine the effects of both photolithography and etch parameters on via profile. Post-exposure bake temperature, lower electrode power, source power, pressure, chuck temperature and gas flows were explored. The responses were via top diameter, bottom diameter and length of vertical sidewall. The sidewall angle was calculated from the top and bottom via diameters for single-sloped profiles (Fig. 2-left). The results revealed that a lower post-exposure bake temperature was the main effect to produce a narrower upper via diameter. A 20°C increase in post exposure bake temperature increased via diameter by approximately 15 microns. The bottom via diameter was not affected by any etch or photo parameters. The angle of the fully-sloped via was calculated to be 75 to 85 degrees. A fully-sloped via with no sharp corners improves the penetration of wet chemistries during the veil removal. A clean, fully-sloped via shape also allows for improved step coverage and thinner metal coatings thus, reduced cost (Fig. 2-left).

Surface profilometry was used to calculate the etch rate and selectivity of the etch process. Step-heights were measured on GaAs wafers patterned with photoresist without a post exposure bake step. The optimized etch rate conditions yielded an etch rate of 5.7 μm/minute. Therefore, the new etch process produced a fully-sloped via profile. Also, experiments with amount of overetch showed the shorter the overetch reduced the amount of veils (Fig. 3).

Figure 3 SEM image of New Via prior to Cleans Processing

VEIL ANALYSIS

Veil formation and composition was highly dependant on the plasma etch processing conditions. Dry etch residues or veils tend to be very complex and difficult to remove because they are made of the by-products of the etch process (the same thing you are trying to etch is being re-deposited in the form of veil material). So, if a photoresist mask is used, the carbon components from the mask become intertwined with other etch by-products. To understand the composition of the veils further, energy dispersive spectroscopy (EDS) and AES were performed. The AES analysis showed the veil was complex with organic and metallic components. The analysis taken after the etch process showed the presence of carbon, oxygen, gallium, arsenic, and gold (Fig. 4-left).

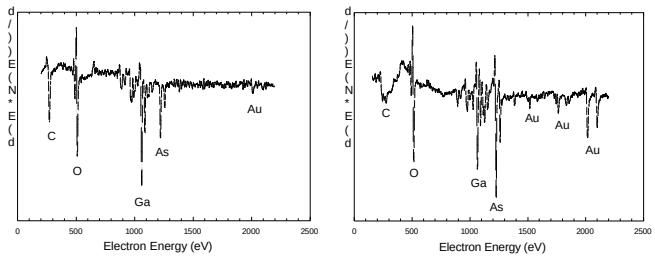

Figure 4 AES Survey of Sidewall Polymer after Plasma Etch Process (left) and after plasma ash (right)

Since we were also interested on the affect of the plasma ash process on veil formation, AES was completed on an additional wafer following ash (Fig. 4-right). From the AES survey, the gold intensity was noticeably increased on the veil surface with plasma ashing. The purpose of the ash is to remove the photoresist from the wafer surface, but the gold etch stop is exposed. The high power plasma that is removing the resist is also bombarding the gold etch stop, causing the gold to be back-sputtered onto the veil surface. Therefore, the increased concentration of gold was theorized to be due to the ash (Fig. 5). This analysis lead to the belief that it may be easier to clean the veil prior to the reactive ion etch (RIE), low temperature ash process.

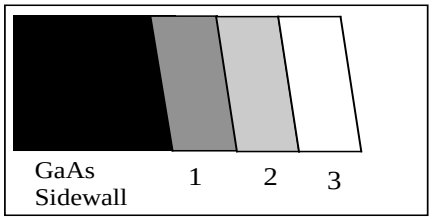

Figure 5 Diagram of Veil Components where layers 1& 2 are from the etch process and layer 3 is from the ash process. Layers 2 & 3 have high concentrations of gold.

As in the evaluation of the etch process, SEM images were taken at a 30 degree angle to give a clear view of the via sidewall. Viewed at various magnifications, presence of veils could be determined. Images were taken after etch processing and post-cleans experiments to determine the effectiveness of each clean process (Fig. 3). Optical microscopes were also used at high magnifications to gain quick previews of clean effectiveness.

VEIL CLEANING

With the new etch process and elimination of the RIE ash process; an attempt was made to look at different veil removal chemistries. The clean process must completely remove the veil without extensively attacking the via profile, etch stop, interfaces, or adhesive. Acids, bases, and oxidizers were evaluated in some combination, but reacted with the thermoplastic adhesive or were very difficult to control Galvanic reactions and GaAs etchrates. Most solvents had a similar response in quickly attacking the mount material. Working with General Chemical Corporation, a series of studies using various chemistries were conducted to determine the best chemistry for the removal of the sidewall residue.

Following the plasma etch, a dilute gold etch step was implemented to remove the back-sputtered gold from the surface of the veil. The optimization of the dissolution process was completed by a simple design of experiments (DOE). From the DOE, the leaching step was increased by 30 seconds providing consistent removal of the surface gold independent of the amount of overetch.

Following via etch and the dilute gold etch, a spray-process tool was used to simultaneously remove the resist mask and post-etch residues. The process with the GenSolve™ chemistry that could be achieved in minutes replaced the lower throughput ash process. The time to strip the photo resist mask was reduced by more than 80%. Also, this process was implemented on fully automated tools as desired for high volume production. The process utilized an automated two-step process, namely, stripping and rinsing. The GenSolve™ chemistry incorporates a balance of solvents, complexing agents, and inhibitors. The rinse step utilized the GenClean™ chemistry allowing penetration into the vias and lifting of loose particles left from the strip process.

During cleaning, by-products of DNQ-novolak present in the mask and veil are rapidly hydrolyzed to more soluble forms. The solvent blend is designed to aid penetration, gel formation, and removal pursuant to a fundamental dissolution model.[6] Dissolution may be inhibited by high concentrations of metallics in the etch residue and a carbonized "skin" on the photoresist surface.[7] Reactive agents in GenSolve™ leach and coordinate components in the veil, including As and Ga, rendering them soluble for rinsing. Selective inhibitors are added to minimize electrochemical etching at the etch stop interface.[8] The chemical formulation allows stripping and veil removal with negligible impact to the thermoplastic adhesive.

Although a simple DI rinse may produce desired results in conventional resist stripping, the removal of dissolved solids and particulate from complex geometries such as a vias required a formulation like GenClean™, which is designed to emulsify dissolved polymer, prevent redeposition, and maintain a reduced surface tension. The effect of emulsification and redeposition is quickly demonstrated by measuring turbidity (cloudiness) of polymer in various process solutions. Table 1 indicates turbidity as a measure of insolubility for a 5% (v/v) of GenSolve™ added to the rinse. To best model the rinsing of a stripping process, GenSolve™ is loaded with the cured-form of a common positive-tone resist (DNQ-Novolak) at various concentrations.

TABLE 1.
Effect of turbidity upon rinsing. GenSolve™ is loaded with resist.

Rinse Agent	0.5% Resist	1% Resist	10% Resist
DI Water	Turbid	Turbid	Turbid
GenClean @ 5%	Clear	Turbid	Turbid
GenClean @ 20%	Clear	Clear	Turbid

Turbidity suggests insolubility of the dissolved solid, in this case, a DNQ-novolak resist. As the solution becomes turbid, the dissolved species forms a suspension, which may redeposit, especially in irregular geometries such as vias.

Penetration and solids removal are best achieved through reduced surface tension and agitation. Particles are held to surfaces by capillary action, electrostatic attraction, or both. Particle removal requires a reduction of energy by minimizing contact through surface tension reduction.[9] As particle size reduces, say, from 1 μm to 0.1 μm, the energy required to remove it will increase by at least a factor of 10. This is explained through geometric equations where mass is related to volume. To overcome this increase, energy in the form of agitation as spraying, sonication, or mixing must be used.

Throughout the process, surface tension must be maintained at reduced level. The choice in strip and rinse chemistry will

directly affect the resultant surface tension of the system. A model of the rinse process is shown in Figure 6.

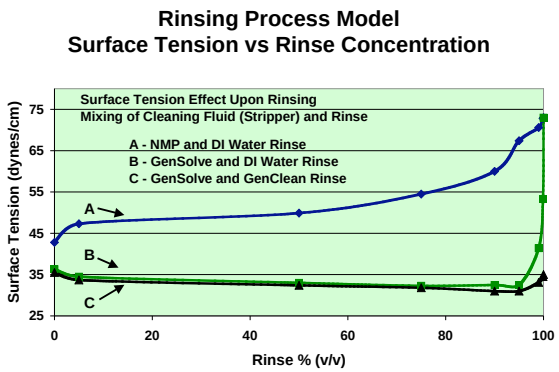

Figure 6 Surface tension effect upon rinsing. Various test solutions: A) Common solvent (NMP) rinsed with DI Water, B) GenSolve™ rinsed with DI Water, and C) GenSolve™ rinsed with GenClean™.

The surface tension of a common resist stripper such as NMP (n-methyl-2-pyrrolidone) will continue to rise when rinsed with water until all of the solvent has been mixed and removed. GenSolve™ is formulated with surfactants to aid in rinsing. Upon mixing with DI water during rinsing, surface tension reduces. Surface tension does not rise until the water rinse reaches greater than 90%. When rinsing with GenClean™, surface tension never appreciably rises. Again, emulsification and low surface tension character are needed with agitation for effective rinsing of dissolved solids and particles. After a dump-rinse or other DI water immersion, residual GenClean™ is easily removed from the surface leaving the vias ready for drying.

One process optimization looked at the effect of the amount of over etch at the through substrate via etch on via cleanliness. This experiment provided the assurance that the vias would remain clean within normal process variations. The final via is shown in Figure 7.

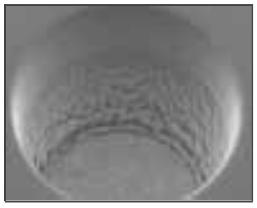

Figure 7 Fully-sloped and veil free via

CONCLUSION

Through a series of experimental designs, a through substrate via etch process was developed. The process yielded a fully-sloped via profile with an angle of incidence of 75 to 85 degrees. The amount of veil material produced was reduced. The plasma ash process was removed, allowing for easier removal of veil due to decreased gold concentration. The veil clean process that was developed utilized a combination of solvent formulas (GenSolve™), a pre-rinse (GenClean™), and a short metal leaching step. The optimization produced a module that was manufacturable and yielded consistently clean vias.

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