Back-side processing poses tough challenges for GaAs

Henry Hendriks, Bharat Patel, Jim Crites and **John Moore** explore the challenges of back-side processing and the developments under way to turn wafer thinning, via hole etching and back-metal deposition into high-yield and high-throughput processes.

Back-side processing of GaAs wafers includes all of the manufacturing process steps beginning just after final front-side electrical test through to die separation and packaging. Detailed reviews of GaAs wafer back-side process flows have recently been published (H Hendricks *et al.*; L Klingbeil *et al.*; C Varmazis *et al.*). The ...le process flow of a typical GaAs fab can be separated into two major branches. The first branch is for GaAs die that do not require back-side via holes or metal. The main process steps involved are wafer thinning, dicing, die inspection and packaging. The second branch is for die that require back-side metal and, in most cases, through substrate via holes. This branch involves several additional process steps, including wafer/carrier mount, back-side photoresist mask definition, via hole etch, photoresist strip, oxygen plasma clean, seed layer deposition and electroplating.

The yield at back-side is crucial to the success of a GaAs fab, as a considerable investment has already been made in front-side processing. Also, major challenges exist in scaling up from 4 to 6 inch diameter wafer platforms. Fab equipment vendors over the past couple of years have taken notice of the growth in demand for GaAs-based devices for wireless applications, and they have started to address some of the tool deficiencies that previously existed in a few of the main back-side process steps. In the current market conditions fab process engineers and managers ...fully reviewing cost-of-ownership ...of tools, while at the same time investigating the use and compatibility of innovative materials and unique process designs.

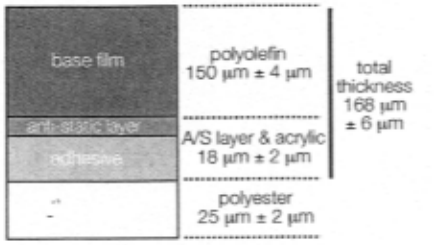

Fig. 1. A cross-section of Ultron Systems' ultraviolet anti-static tape.

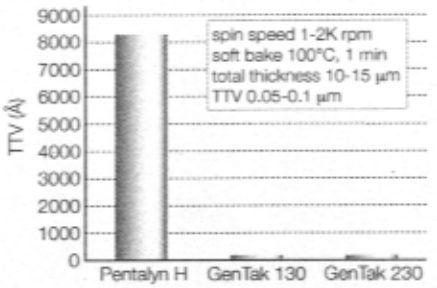

Fig. 2. The total thickness variation (TTV) of three cured spin-on adhesives.

This attention to back-side processing will certainly result in creating simple and robust developments that can be easily ramped during the next market rebound.

Process flow for thinning on tape

For 6 inch diameter wafers that do not require vias and back-metal, an ultraviolet (UV) back-grinding (BG) tape is generally used to protect the wafer front-side (figure 1). If the wafers have air-bridges, a thick photoresist can be applied to protect them during the tape mount and subsequent thinning steps. For high-volume manufacturing, an automatic wafer taper and de-taper with a UV exposure module are typically used (P Heinze, J Muller *et al.*). On UV exposure the adhesive layer strength of the tape is reduced to between 1% and 5%. The UV BG de-tape step should be carried out after the thinned wafers have been mounted on dice tape frames, so that thinned wafers are continuously supported by tape base film from the grind-through dice steps. Wafer tape system vendors are developing automated tools that combine the UV BG de-tape step with the dice tape frame mount step, which are targeted for smart card applications and may soon be available for use on 6 inch GaAs wafers. Some GaAs fabs have recently shown that 6 inch wafers with UV BG tape can be thinned with high yield to a target thickness range of 250–125 µm.

An automated single-wafer/dual-spindle grinder is used to perform most of the wafer thinning, which is followed by a post-grind wet etch or polish to remove the grinding damage layer. The dual-spindle grinder performs a fast, bulk, rough grind followed by a slow, thin, fine grind to achieve high throughput and to minimize the thickness of the grinding damage layer. A spray etch or polish is typically done after the grind to remove the grinding damage layer. Some wafer-thinning vendors offer a single wafer spray etch or polish module as an option for the automated wafer grinder system.

Process flow for vias and back-metal

For wafers that require vias and back-metal, the wafers can be thinned to between 100 and 20 µm. This requires the wafer to be mounted on a carrier using a high-temperature wax, thermoplastic adhesive or heat release tape. Liquid thermoplastic adhesives can be applied using a coat and bake track while dry-film adhesives can be applied using a dry-film vacuum laminator. Perforated sapphire carriers are currently used for 6 inch wafer processing. However, new automated wafer/carrier mount and demount tools may allow for the use of non-perforated carriers. Doped borosilicate glass carriers with a thermal coefficient of expansion close to that of GaAs are being considered as a less expensive alternative to sapphire with a potential cost saving of up to several hundred dollars per carrier.

Maintaining substrate planarity and a tight total thickness variation (TTV) is crucial during wafer-to-carrier mounting, especially when trying to achieve very low target thickness. Liquid spin-on thermoplastic adhesives tend to offer tight TTV, although variations do exist depending on the product used (figure 2). Pentalyn H, a customer's spin-on prepared with resin from Hercules, and GenTak, a

ready-to-use dual polymer system from al Chemical Corporation (GCC), were spun and baked onto 6 inch GaAs wafers for a 10 µm target thickness and were shown to have a TTV of nearly 10% and 0.03% respectively. GenTak is available in a variety of viscosities, offering flexibility in the application to wafer front-side surfaces with a range of topography and thickness requirements (figure 3).

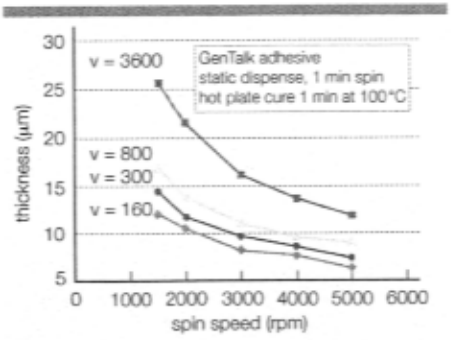

Fig. 3. Spin curves for several different values of viscosity (v) of GenTak liquid adhesive.

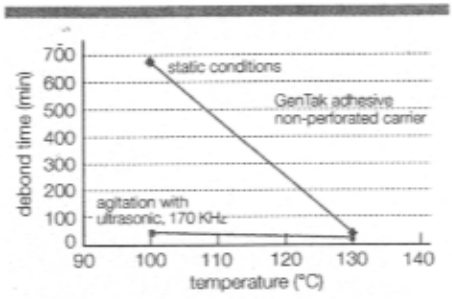

Fig. 4. Demount process parameters for static conditions and ultrasonic agitation.

Via hole etch and metalization

High-density plasma etch tools based on inductively coupled plasma (ICP) and dual frequency enable single 6 inch wafer via etch processing with high throughput, even for individual source vias (ISVs) which fit within 30 µm front-side source pads of power FET devices. This subsequently allows better heat conduction away from the hot active regions of the device. For high-aspect-ratio ISVs, long-throw or collimated sputter deposition may be required to ensure conformal seed layer deposition through the vias. Some 6 inch fabs with ISV capability have gone to a cluster platform with individually configured chambers. However, for fabs with less stringent via aspect ratio requirements, an auto- batch sputter system can be used for seed layer deposition.

Wafer electroplating systems with pulse capability and carefully engineered solution circulation, such as fountain or submerged eductor-type platforms, are being used to deposit a conformal thick gold layer (3–8 µm) onto the back-side surface and through the vias. If the die are to be attached to package carriers for module assembly using a high-thermal-conductivity epoxy, then a solder-stop layer inside the vias is unnecessary. If the die are to be attached using Au-Sn eutectic solder preforms, then a solder-stop metal that readily oxidizes, such as Ti, TiW, Ni or Cr, needs to be deposited by either sputtering or plating inside the vias to prevent solder from blowing out the front-side metal pads.

A photolithography/wet-etch process is typically used to clear the solder-stop from the back-side metal plane to minimize voiding at this interface during the die-attach step. For large via openings at the back-side surface, the thick, positive photoresist flows into and fills the via during the dispense step. This enables a flood exposure and develop process ed after back-side dicing streets have efined saving one contact mask step. During the resist bake step, it is possible for some solder-stop metal to diffuse slightly into the thick gold layer along grain boundaries. This small concentration of diffused metal can later oxidize and create voiding problems at the solder die-attach step. A quick fix is to implement a short gold wet etch (potassium iodide or cyanide based) to lift off the solder stop metal embedded in the grain boundaries. Finally the resist mask can be wet stripped.

With recent advances in robotics, vendors can now offer fully automated pick and place, hot-forming gas die bonder platforms.

Thinned wafer demount and dicing

The thinned wafers can be demounted from the perforated carriers utilizing specially designed demount cells and a multi-bath solvent system at elevated temperature with agitation. BPS Technologies has recently introduced a semi-automated solvent hood with special vacuum holders to handle the thinned wafers after the carrier has been released from the wafer. The thinned wafers are subsequently released from the vacuum holders into a special cassette while they are submerged in liquid. EVGroup and BLE have recently introduced automated wafer demount tools with special thin wafer handlers that can be used with non-perforated carriers. Also, GCC has shown that it may be possible to demount and clean 6 inch thinned wafers from non-perforated carriers in just a few minutes using GenSolve 500. When heated to elevated temperatures with high-frequency, low-power ultrasonic agitation, wafers can be demounted without damaging front-side gates and air-bridges (figure 4).

Dicing of thinned wafers less than or equal to 100 µm thick may require the use of UV dice tape, especially if the wafers are to be sawn. The structure of UV dice tape is very similar to that of UV BG tape (figure 1, pXX). On UV exposure, which is recommended within 24 h after the wafer is mounted, the adhesive strength of the tape is decreased by almost two orders of magnitude, enabling thin, fragile die to be picked and placed from the dice tape.

Au-Sn eutectic solder die attach

Most GaAs device-die with back-metal are attached to packages or module carriers using conductive thermoset epoxy. However, for high-power devices a Au-Sn eutectic solder with a melt temperature of 280 °C may be needed to satisfy the thermal conduction requirements between the active region of the device and the heat sink. With the recent advances made in robotics, vendors can now offer fully automated pick and place, hot-forming gas die bonder platforms. For high power devices that need to be die attached using Au-Sn eutectic solder, a smaller die size is desired to achieve a more robust die attach process. A void-free die attach may be required to ensure the adequate thermal conduction of heat away from the power amplifier active regions. For the pick and place die bonders, larger die typically require a higher forming gas flow to promote an increased heat-transfer rate and to reduce voiding between the solder preform and die back-metal surface. Also, a programmed scrub is needed to break down the tin oxide on the preform prior to the forming gas flow.

C-mode scanning acoustic microscopy (C-SAM) can be used as a periodic screen test to check for excessive voiding between the die and carrier after die attach, and it is also useful in optimizing a die-attach process. The package or module needs to be submerged in DI water, so the test can be destructive if it is non-hermetically sealed. C-SAM images of three Au-Sn eutectic solder preform die

attachments done with a pick and place, gas ...der are shown in figure 5. The first die ...ach was essentially void-free because tiny voids occurred only at the vias, which are lined with solder-stop metal. The second die attach had a few large voids as a result of residual solder-stop metal on the die back-metal surface. The third die attach showed a very large void due to the partial wetting of the preform, which was traced to misalignment of the forming gas nozzle.

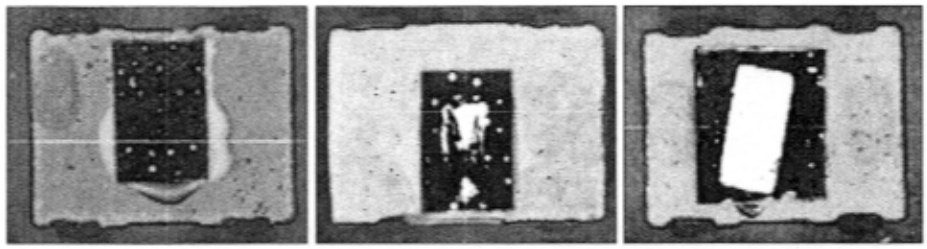

Fig. 5. C-SAM images of void-free and void-problem Au-Sn solder preform die attach. Voids are white. Left to right: good die attach; residual solder-stop metal; gas nozzle mis-aligned.

Depositing Au-Sn directly onto the backside of the wafer is being explored as an alternative to the use of Au-Sn eutectic preforms stamped to accommodate specific die sizes. The Au and Sn can be deposited either sequentially or jointly to try to achieve the eutectic composition needed for die attach. Also, a Au "sealcoat" layer can be deposited to prevent the Sn from oxidizing before or during the die attach. This should lessen the demands on the scrub and hot forming gas flow steps to reduce surface oxides. The eutectic Au-Sn preform thickness is typically about 25 μm, necessitating the use of a solder-stop layer inside the vias. The deposited Au-Sn layer or total composite layer thickness can be tailored to obviate the need for a solder-stop layer. With the recent advances made in wafer electroplating tools, depositing Au-Sn directly onto the wafer back-side may shortly move from the R&D phase into manufacturing. ●

Further reading

P Heinze 2001 *TAPtechnology* **10(3)** 95.
H Hendriks *et al.* 2001 *GaAs Mantech Digest* 181.
H Hendriks *et al.* (in press) *2001 CS-MAX Conference Proceedings.*
L Klingbeil *et al.* 2001 *GaAs Mantech Digest* 41.
J Muller *et al.* 2000 *Semiconductor International* **23(7)** 191.
C Varmazis *et al.* 2000 *Semiconductor International* **23(14)** 87.

Henry Hendriks, Bharat Patel and Jim Crites work for M/A-COM: Tyco Electronics, Lowell, MA. E-mail hhendriks@tycoelectronics.com. John Moore works in the Electronic Chemicals Group of General Chemical Corporation (GCC), Hollister, CA. E-mail jmoore@genchemcorp.com.