

## Substrate Temporary Bonding Supporting Post-Processing Applications

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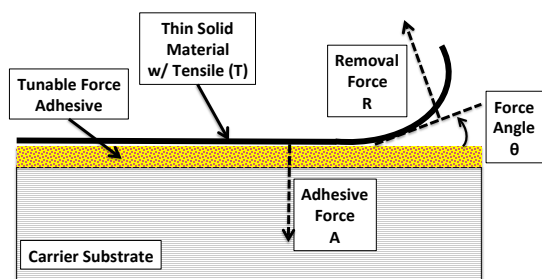
### Abstract

Post-processing applications are carried out on substrates while they are temporarily held in place. This requires a simple adhesion process with easy removal without the burdens of complex tooling or cleaning. Substrates include wafers, flexible displays, or components, organic or inorganic, and may contain topography such as solder bumps. The applications may vary from thinning and backside processing of wafers, complete flexible circuit integration, or the stacking of packages. Simple wafer thinning may use green products as the DaeCoat™ 600-series detergent soluble, exhibiting thermal stability from 80°C to allow hot DIW debond, to over 200°C to support plasma deposition or related processing. Temporary bonding may resist exposure to excessive heat and chemicals for many steps or a simple one-step process. The DaeCoat™ 300-series of products are designed to resist thermal exposures  $\geq 300^\circ\text{C}$  for wafer operations with bumps or reach  $\geq 400^\circ\text{C}$  (DaeCoat™ 315) for flexible displays to allow casting of liquid polyimide (PI) [1]. The properties are consistent with the needs of electronics processes, providing outgas below 1% inert to fab chemicals, and most important, an adhesive force that is tuned to allow simple substrate removal (peeling, lifting, or chemical diffusion). Where discrete die or components require installing infrastructure to support stacking or fan-out designs, the thin and fragile substrate is securely held in place by simple dry bonding completed in seconds and later removed by similar peeling practices without observed residue. Such component practices enable encapsulation during bumping, permanent bonding, or vacuum deposition of EMI/RFI shielding [2]. The success in these and other technologies depend upon the use of the proper adhesive but most importantly, the tuning of the adhesion force. Successful tuning depends upon many factors, including substrate surface energy, texture, and the bonding process. Daetec has created adhesives used in temporary bonding processes for nearly 20yrs, applying to multiple wafer types, OLED and TFT displays, printed electronics, solar, thinning down to 4um, and thermal resistance  $>600^\circ\text{C}$  [3]. Our experience in creating solutions for these and other industry needs will be discussed as well as the criteria to temporarily support flexible and rigid substrates of all types, sizes, and shapes.

Key words: adhesive, temporary bonding, de-bonding, carrier EMI/RFI shielding,

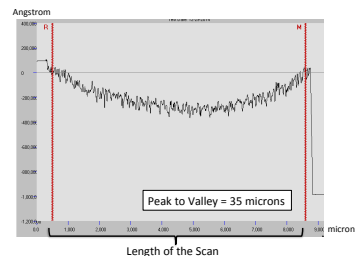
### I. INTRODUCTION

Effective temporary bonding is achieved by understanding the substrate and modeling the forces at play during the process and at de-bonding. (Fig. 1).



**Fig. 1:** Modeling temporary bonding with tensile (T), adhesion (A), removal (R).

When creating a temporary bonding process, de-bonding by peeling, sliding, or pulling is best defined early. Knowledge of your substrate, its thickness, texture, chemistry, and in some cases, bow/warp is critical to success (e.g. package sealing in high vacuum PVD processing, Fig. 2).

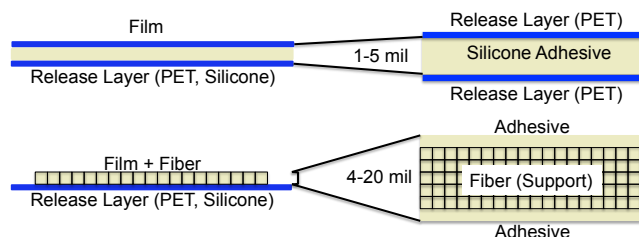


**Fig. 2:** 35um warp of electronic LGA packages.

Processing thin and fragile parts requires de-bonding that transfers parts from one medium to another without sacrifice to their integrity and at minimum total cost of ownership. In theory, these concepts appear sound, while common experience uses practices that are overkill. Often the result is complex with lengthy temporary bonding measures that drive up costs and reduce yield. This paper is intended to challenge the reader to expand their awareness of their substrate and process needs while exploring new possibilities in temporary bonding.

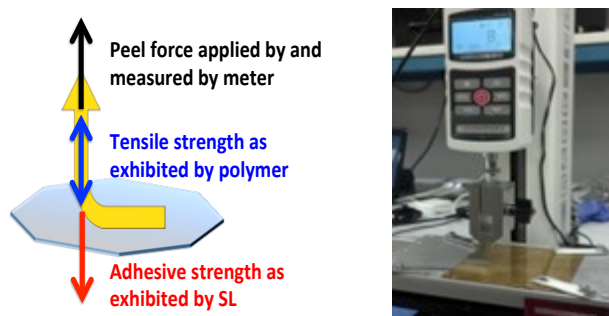
#### A. Tape Adhesives

A variety of tape products exist, the most common being pressure sensitive acrylics (PSAs). Silicone may be chosen for thermal resistance. Both of these tapes are produced in a range of forms, namely, transfer tape, single sided, and double-sided. The transfer tape is created as adhesive sandwiched between two release layers. Single and double-sided are manufactured with adhesive applied to one or both sides of a backing, respectively. For desired uniformity, polyester (PET) is chosen as the release layer and backing. Where high temperature processing is desired, polyimide (PI) is chosen as a backing over PET. Examples of tapes created at Daetec range from thermoset silicone to thermoplastic composites (Fig. 3).



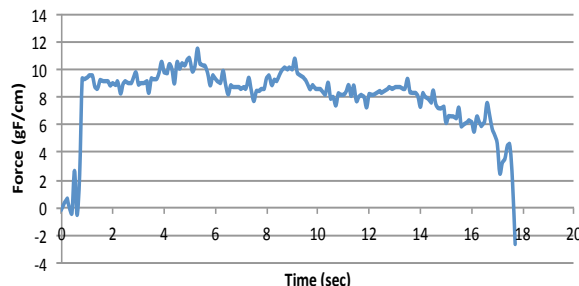
**Fig. 3:** Silicone transfer (above) and composite (below) tapes with PET release layers, 1-5mil (25-125um) and 4-20mil (100-500um), respectively.

Adhesive force is measured by a peel mechanism, ASTM D3330, with system set-up using a digital load cell and tests in a 180° or 90° orientation using a sled. A range of polymers and backings may be tested as a physics problem where sufficient force exceeds the material adhesion under the tensile strength of the backing (Fig. 4).



**Fig. 4:** Vectors showing set-up of adhesion test.

Adhesion tests are important to evaluate minimum bonding needs (adhesion tuning) for a process while allowing a range of de-bond options to be exercised. Adhesion force plots similar to those shown (Fig. 5), are evaluated, averaged, and presented to understand performance during a wide range of conditions.



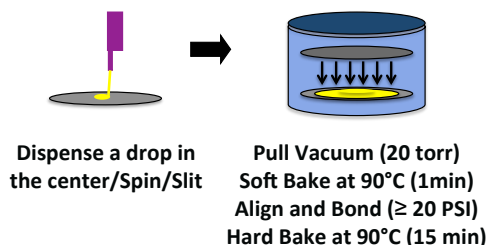
**Fig. 5:** Adhesion force measurement.

While adhesive tapes may offer convenience, they have limitations and are more costly as compared to liquid applied systems. While some exceptions exist, the minimum adhesive thickness in PSA and silicone tapes is ~1mil (25um). Increased costs for tape form adhesives are based upon the added material backing and release layers for manufacturing and handling.

#### B. Liquid Adhesives

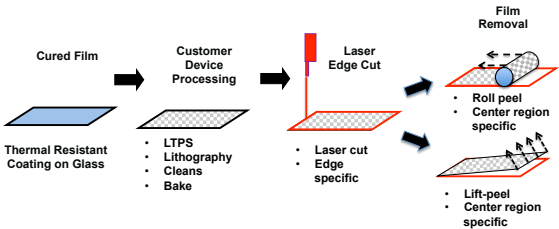
Adhesives in liquid form may be cast through an evaporation process, hot melted, or cured by crosslinking by heat and photo exposure. For temporary applications, there is commonly two different substrates that require bonding, namely a device substrate and a carrier. The carrier is a dummy or “handle” that supports the thin fragile device substrate during processing. Liquid adhesives are commonly applied to the device wafer as there may be exist topography that is desired to be planarized. Once the adhesive is applied, one of two options may proceed, a wet-bond or a dry-bond.

**Wet Bonding.** Adhesive is applied to the device substrate, followed by a soft-bake, and bonding to the carrier using thermal processing to initiate cure. A range of polymers have been reported for wet-bonding of wafers, including rosin-urethane [4], silicone [5], rubber [6], and acrylic [7]. A typical process flow is given. One product used for wafer or smooth substrates is DaeCoat™ 365 (Fig. 6).



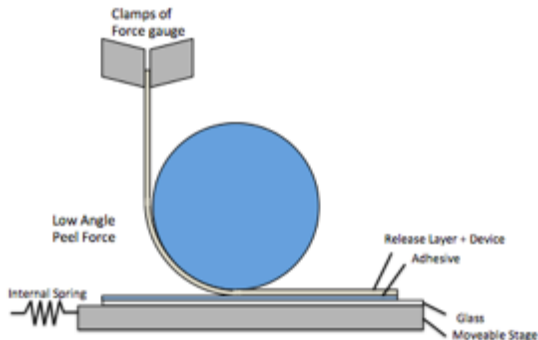
**Fig. 6:** DaeCoat™ 365 wet-bond process flow.

Flexible displays commonly use PI as the substrate whereby the electronic circuit is built. To minimize irregularities, many choose a liquid polymer and cure directly onto the carrier. Applying DaeCoat™ 315 prior to PI coating ensures a secure bond, yet allows release on-demand without damage. Release may be conducted by a variety of means to include peeling and lift-off, much desired mechanisms as compared with laser de-bond (Fig. 7).



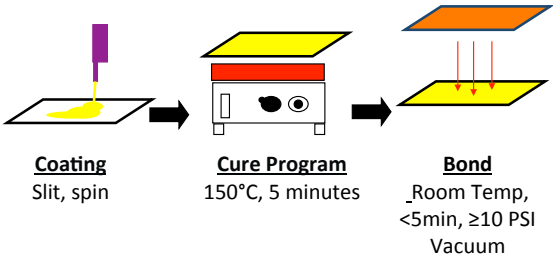
**Fig. 7:** DaeCoat™ 315 flexible display process flow.

The adhesive layer of DaeCoat™ 315 is very thin, usually 0.25um (250nm), ideally suited for conditions of high uniformity and control. Tuning of adhesion force is fundamental. The work unit (PI layer) is not cleaned as the adhesive remains on the glass carrier allowing for HVM recycling back through the line for bonding to another work unit. While many options exist for de-bonding, an example of a roll-style tool is shown whereby external force and its angle (R & Ø, Fig. 1) are controlled (Fig. 8).



**Fig. 8:** Example of a flexible display removal tool.

Dry Bonding. Adhesive is applied to the device substrate, fully cured, and is immediately brought into contact to the carrier using pressure to bond. Benefits of dry-bonding include a room temperature bond, an effort to reduce thermal-driven bow/warp of the bonded stack. Several versions of dry bonding exist for spin or spray applications where the substrate may vary from a wafer, thin polyimide film, or thick but irregular electronic LGA or BGA packages. The carrier substrate can take on different forms according to the engineering design of bond and de-bonding. DaeCoat™ 355 is a dry-bond temporary adhesive, applied by spin or spray, resulting in a “coated tape” from 1-500um (Fig. 9).



**Fig. 9:** DaeCoat™ 355 dry-bond process flow.

### C. Properties of Adhesives

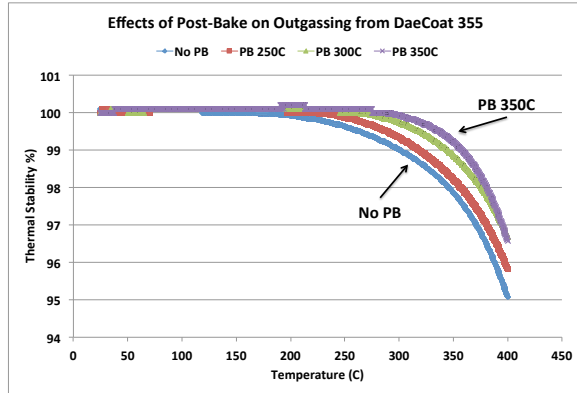
While there are many formulary knobs to turn that control the properties of an adhesive, fundamental aspects of the process should first be addressed. For example, while tape adhesive appears to be convenient, it has serious limitations in thinning wafers below 100um. The elasticity and thickness ( $\geq 1\text{mil} = 25\mu\text{m}$ ) are too high. Therefore, it is important to start by categorizing temporary bonding according to the process (Table 1).

Table 1. Adhesion properties according to the needs of application and process.

Application	Modulus	Adhesion	Thermal	Uniformity
Mechanical (e.g. thinning)	↑	↑	↔	↑
Vacuum (i.e. PVD, plasma etch)	↔	↔	Tool dependent	↔
Dielectric cure and/or material anneal	↔	↔	↑	↔
Full process:				
Thinning + backside Process + PI curing	↑	↑	↑	↑
Flexible display (poly-Si anneal)	↔	↔	↑	↑
Pkg EMI Shielding (low temp PVD)	↔	↔	↔	↔

In Table 1, adhesion properties are sorted according to application (i.e. mechanical, vacuum, etc.) and process. For example, a wafer thinning process requires high performance on all adhesive attributes, which may include dielectric (PI) curing. Alternatively, EMI shielding may include simple form adhesives.

Thermal and chemical resistance. Temporary bonding technologies created for the electronics market must be resistant to common processes in the fab. To this end, Daetec’s products meet minimum thermal resistance to 300°C exhibiting <1% outgas (non-detectable) and chemical resistance to common chemicals used in manufacturing; DaeCoat™ products (Fig. 10, Table 2).

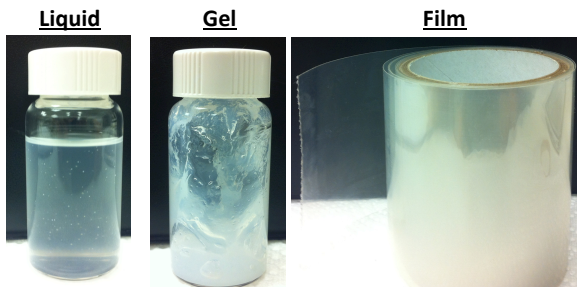


**Fig. 10:** DaeCoat™ 355 in oxygen/air; (>450°C (inert).

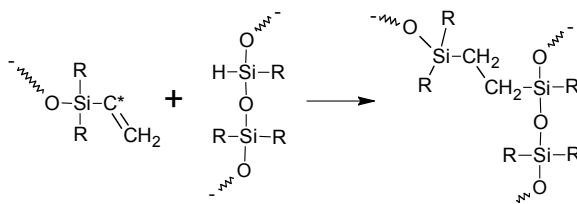
Table 2. Chemical resistance of DaeCoat™ products.

Chemical Exposure (@ 25°C)	Time (min)	Effects
Phylic organic solvents as: NMP, DMSO, PGMEA, Acetone	30	No Attack
Aqueous developers as: TMAH, NaOH, KOH	30	No Attack
Organic acids as: CH <sub>3</sub> COOH	30	No Attack
Mineral acids (dilute): H <sub>2</sub> SO <sub>4</sub> , HNO <sub>3</sub> , HCl, H <sub>3</sub> PO <sub>4</sub>	30	No Attack
Common formulated PR strippers: EKC, DMSO/MEA, Fuji, TOK	30	No Attack

**Delivery forms & reactivity.** Success in temporary bonding process depends upon the ability to deliver adhesive in range of forms. DaeCoat™ products are available in liquid, gel, and film (Fig. 11), utilizing thermal and UV curing, including a highly efficient silicone (Fig. 12).



**Fig. 11:** DaeCoat™ adhesive forms.

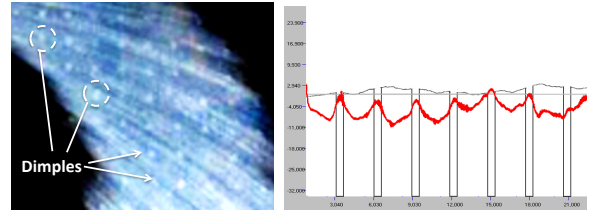


**Fig. 12:** Clean & efficient vinyl silicone curing.

#### D. Carrier Designs

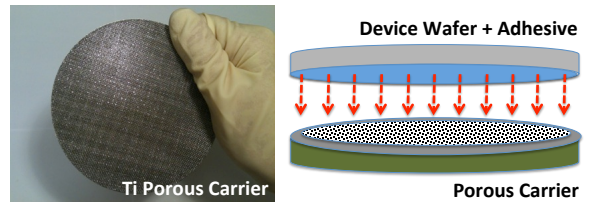
The temporary bonding design must consider the nature of the carrier and how it interacts with the adhesive and device

substrate to produce a reliable process. Daetec works with every substrate available to create engineered carriers. Such carriers support the process and de-bond on-demand. Porous carriers perform in this manner without the irregularities as dimples caused by perforations (Fig. 13), increase the release rate (i.e. 15min), and most important, are scalable to virtually any diameter (300mm, 450mm).



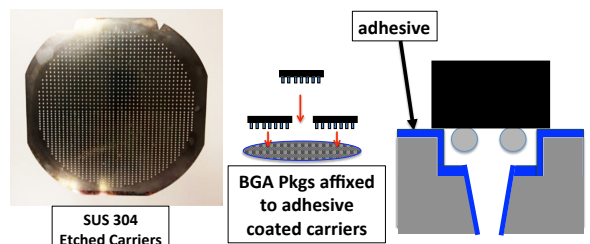
**Fig. 13:** Dimples observed ~0.5um (~5,000 Å) on a Si wafer from a perforated sapphire carrier of a 50um grind.

Porous carriers include a Ti-based composite, created to achieve desired thin substrate uniformity (TTV <2um) when processed to 50um. The carriers de-bond in 15min at RT when using the dry-bond DaeCoat™ 355 and DaeClean™ 300 cleans (Fig. 14).



**Fig. 14:** Porous carrier created from Ti metal.

Further work continues in creating carriers for temporary bonding, including for electronic packages (Fig. 2). Stencil and 3D etched metal carriers temporarily affix parts while they are processed in a vacuum chamber. Adhesive is applied to specific landing areas on the carrier to affix the parts while sensitive topography is undisturbed (Fig. 15).



**Fig. 15:** Metal carriers for BGA temporary bonding.

## II. EXPERIMENTAL

### A. Materials

For process demonstration and testing, remanufactured silicon substrates at diameters of 100-200 mm (4-8") of known crystal orientation and thickness (1-0-0, ~525 μm;



Wollemi Technical, Inc. Taiwan, [www.wollemi.com.tw](http://www.wollemi.com.tw)). Materials used include those items stated in Table 3 [8]. Process chemistries include: TMAH (0.26N), isopropanol (IPA), n-methylpyrrolidone (NMP), various dilute mineral acids, and sulfuric acid copper plating bath. Tape products include those manufactured by Daetec.

Table 3. DaeCoat™ products in various applications.

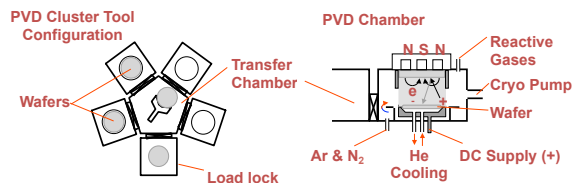
Work Unit	Market	DaeCoat™	Method
Dry Film (organic PI or metal foil)	OLED, organic printed circuits, flexible displays	355 (dry-bond)	Coat & cure on glass carrier, bond w/pressure
Liquid Casting (PI liquid)		315	Coat & cure on glass carrier, cast & cure liquid
Thin glass	TFT LCD	355 (dry-bond)	Same as above
Wafer	3DIC	355, 365, 615, 625	Coat & cure on device wafer, bond w/pressure
Die (chip)	Package	355	Cure on carrier, bond w/pressure

### B. Equipment

Coatings are produced on a Brewer Science, Inc. CB-100 spin-coater, while spray and encapsulation uses custom tooling designed at Daetec. Metrology data is generated by a XP-1 stylus profiler [9]. Bonding and de-bonding equipment is designed at Daetec. Adhesion is performed on Mark-10 equipment (<http://www.mark-10.com/>).

## III. RESULTS

Experiments are performed to demonstrate different temporary bonding practices for wafers, displays, and device packages. These processes require high vacuum conditions, reaching  $10^{-7}$  T near 200°C. Glass substrates were coated and cured with DaeCoat™ 355 using normal application guidelines and no extra outgassing measures. The samples were shipped to Tango Systems, Inc. [2] for vacuum tests, configuration and results are shown (Fig. 16).

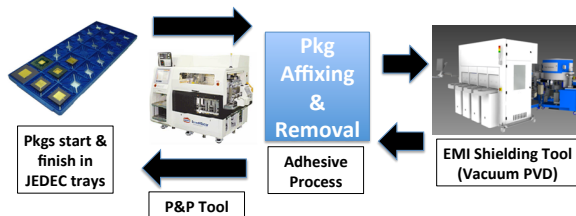


PVD Condition	Pressure (e-7)
Chamber only	1.6
Chamber + open-face sample	6

**Fig. 16:** Vacuum process configuration testing using a PVD system designed for EMI shielding. [2]

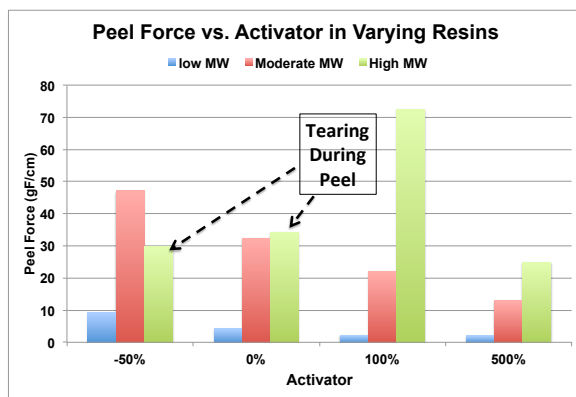
### A. EMI/RFI Shielding of LGA/BGA Packages

DaeCoat™ 355 adhesive is used to affix land grid array (LGA) and ball grid array (BGA) packages onto carriers prior to being processed by PVD. The HVM process uses a P&P tool transferring parts between trays, carriers, and PVD system (Fig. 17).

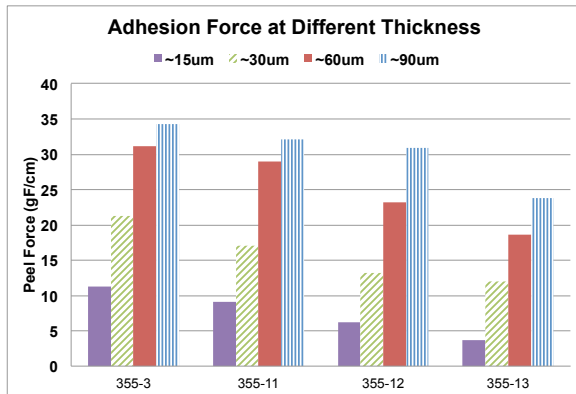


**Fig. 17:** HVM process for PVD EMI/RFI shielding.

Success in the affixing process is based upon thermal stability, no sidewall creep, no under-side deposition (back spill), and no residue. The product must accept a bow/warp of the component at >30um (Fig. 2). Low profile LGAs conform to adhesive whereas the high standoff in BGAs ( $\leq 300\mu\text{m}$ ) create challenges that require a special carrier (Fig. 15) [2]. Etched or “pocket” carriers accept BGAs with proper adhesive placement. Varying technologies in adhesive placement requires tuning physical properties such as adhesion and thickness (Figs. 18 & 19).



**Fig. 18:** Adhesion vs. resin MW in DaeCoat™ 355.

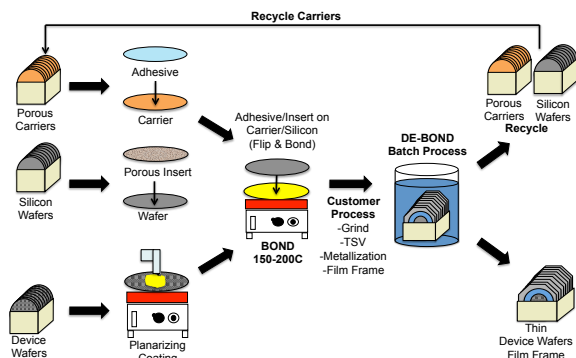


**Fig. 19:** Adhesion force increase with thickness.

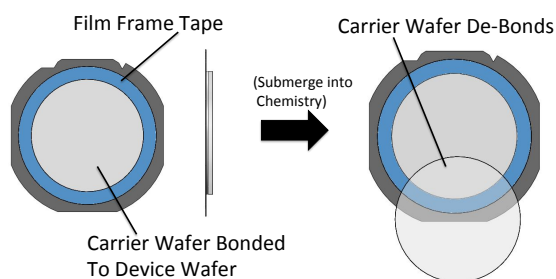
Adhesion force increases with MW of the resin that can contribute residue (Fig. 18) and also rises with thickness that allows greater surface wetting with a given contact pressure during bonding (Fig. 19).

#### B. Dry-Bonding for Wafer Processing

As described in Sec. 1.B.Dry-Bonding, a wafer processing adhesive requires extreme performance in all key areas of temporary bonding (Table 1). De-bonding occurs on-demand by special carriers (Sec. 1D) using a capillary driven penetration by DaeClean™ 300. This occurs while the device wafer is supported onto a taped film frame, as described in the technology, DaeBond 3D™, conducted in a low-cost wet bench (Figs. 20 & 21).



**Fig. 20:** DaeBond 3D™ technology flow.



**Fig. 21:** Carrier de-bond from the taped film frame.

Carrier de-bonding occurs in Tank 1 by liquid penetration to break the edge seal and migrates swiftly through the porous coating until saturation causes a drop in adhesion. Cassettes of film frames holding device wafers proceed to tank 2 for final washing, rinsing, and drying.

## IV. CONCLUSIONS

This paper presents early stage concepts in designing processes that require temporary bonding and encourage plans to remain simple. While many plans may meet a desired process there remains a complexity in de-bonding thin and fragile parts. The authors present the value and limitations of simple tape adhesives and more complex options to meet thermal, organic film (polyimide), and substrate thinning requirements. Creating a successful process is based upon matching adhesive with the corresponding substrate and carrier to achieve a process that is engineered to perform within specific boundaries. The concepts have merged to form processes in EMI/RFI shielding of LGA/BGA packages and in wafers (DaeBond 3D™). The concepts presented here are intended to be applied to many other products and markets.

## ACKNOWLEDGMENT

The authors would like to thank the staff at Tango Systems, Inc. for making this work possible.

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- [7] U.S. Patent Applications 2009/0017248 A1 (2009), *Larson et al.*; 2009/0017323 A1 (2009), *Webb et al.*; and International Application WO 2008/008931 A1 (2008), *Webb et al.*
- [8] Spin coatings, adhesives, encapsulants, cleaners, equipment, and processing designs utilizing a wide range of cure approaches including evaporative, photo, and thermal are from Daetec, LLC, [www.daetec.com](http://www.daetec.com).
- [9] Series XP, AFP, and Xi, are contact and non-contact profilometers as produced by Ambios Technology, Inc., [www.ambiosotech.com](http://www.ambiosotech.com).