High Throughput Thin Wafer Support Technology for 3DIC

Jared Pettit, David Young, Alex Brewer, Alman Law, and John Moore
Daetec, LLC, 1227 Flynn Rd., Suite 310, Camarillo, CA 93012 (jmoore@daetec.com, www.daetec.com)

Abstract

The 3DIC market has been underway for several years. As many companies investigate this business, more is understood about the challenges and cost. All existing commercial technologies use a spin-on adhesive applied to the device wafer, bonded to a carrier, and after processing, de-bonded by widely different practices. One of the leading technologies includes WaferBond™, a rubber-based adhesive developed by Daetec and supplied by Brewer-Science, Inc. (BSI).[1] Daetec has developed numerous temporary bonding systems, including a rosin and a silicone, sold under the trade name GenTak™ (formerly General Chemical, now KMG) [2] and a unique carrier that is cured directly to the device wafer and chemically broken down during debond, developed for SUSS MicroTec.[3] At this year's 2013 Semicon-West gathering, a panel of global experts from KMPG, IMEC, Sematech, CEA-Leti, and CNSE were asked to identify the semiconductor industry's greatest technical challenges.[4] Next to lithography, these experts believed the top challenge is to reduce the barriers to 3DIC. Such barriers include: high cost, poor yield, and poor throughput. When only a few companies can afford 3DIC, progress is slow and growth towards >2 integration levels is pushed to the future. Daetec has developed a new technology, DaeBond 3D™, allowing carrier de-bond to occur in a batch process and while thinned device wafers remain affixed to film frames. Other benefits and sample substrates will be presented at the show.

Key words: adhesive, thinning, bumping

I. Introduction

3DIC processes require wafer support by affixing an adhesive bonded carrier to the device wafer. This approach is the most reliable to protect thin substrates and achieve satisfactory chemical and thermal resistance for backside processing. A rigid and supportive carrier enables good surface planarity, low TTV, and reduces both internal stress and wafer bow during grinding [5-8]. The adhesive bonded carrier supports backside processing, including TSVs, metallization, and dicing. The process begins at bonding, one of the two active stages in processing thin wafers, bonding and de-bonding (Fig. 1).

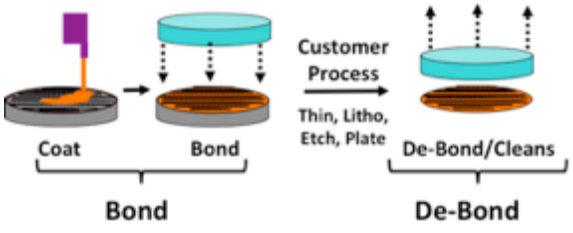

Fig. 1. Two active stages to the use of any temporary adhesive and carrier, bonding and de-bonding.

The choice of adhesive determines the method of de-bonding. Although the current technologies involve an adhesive-carrier support, their chemistry and debond practices. The adhesives are similarly applied yet their debond practices vary widely technologies (Fig. 2).

Table 1. Commercial temporary adhesives.

Supplier	Product	Chemistry	Thermo-reaction	De-bond
BSI	WaferBond™	Rubber	Plastic	Chem. diffusion w/perf. carriers, thermal slide, ZoneBond
3M	LTHC™ & LC-series	Acrylic	Set	Laser assisted debond + peel
DuPont	HD™ 3000-series	Polyimide	Plastic	Chem. diffusion w/perf. carriers, laser ablation
TMAT	Release layer + adhesive	Silicone	Set	Pull-apart
Dow-Corning	WL-series adhesive + release layer	Silicone	Set	Pull-apart
TOK	Zero Newton	Urethane	Plastic	Chem. diffusion w/perf. carriers
DOW	Cyclotene	BCB	Set	Chem. diffusion w/perf. carriers

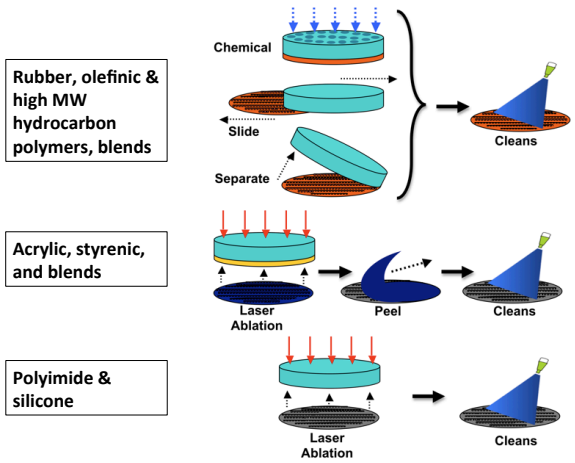

Fig. 2. Variable de-bonding of existing technologies.

De-bonding of the rubber/olefinic adhesive is offered as three choices, chemical dissolution through a perforated carrier, thermal slide, and separation of the carrier by the use of a reduced adhesion layer to an inner region of the carrier that has been previously prepared and masked. An acrylic-based temporary adhesive requires laser ablation of the interface between the carrier and adhesive and once removed, the remaining adhesive layer is peeled away from the thinned product wafer. Other options include the use of polyimide and silicone adhesives, both using a similar ablative removal. All of these technologies require a final cleaning step to remove adhesive residue from the product wafer.

A. 3DIC Challenges

At the time of this publication, one of the top challenges to the semiconductor industry is to reduce the barriers to 3DIC. Such barriers include: high cost, poor yield, and poor throughput.[4] When few companies can afford 3DIC, progress is slow and integration of >2 level stacking is pushed into the future. Several process challenges of the existing technologies are listed below.

Low Yield: Current technologies require physical stress to separate the carrier from the device wafer (thermal slide, peel/pull, laser ablation, etc.). Variable performance exists depending upon adhesive type, wafer size, thickness, device topography, adhesive thickness, carrier condition, process exposure, and the tool operation. These issues produce irregularities that lead to reduced yield.

Low Throughput: Current single-wafer processes must handle the device wafer multiple times as it is moved from the carrier, affixed to a tape film for dicing, and isolated during cleaning. Handling and more tools lengthen the process and drives down throughput. Current processes per tool achieve between 8-12 wafers per hour (wph). The goal of >20 wph is projected as a future plan.[9]

Unsupported Thin Substrate Handling: It is an objective to conduct 3DIC processes with the thinned device wafer "continually supported". Transferring the fragile wafer multiple times between supports is believed to reduce yield.

Cleans Non-Compatibility with Tape: Although it is a desire to finish the process onto a film support, taped film frames are not compatible to most organic solvents. Additional tooling is needed that isolates the tape from the cleaner.

High Tool Cost: Depending upon the technology, wafer size, robot, and modules, single-wafer 300mm de-bond tools are projected to be $1.5-8m. This cost combined with poor throughput and yield makes it cost prohibitive to consider HVM.

Carrier Not Recyclable: Radiation-based separation practices require meticulously clean and transparent carriers. Plasma exposure and handling introduce surface irregularities, affecting laser performance, and hitting yield.

Not Scalable: As projections of 450mm processes start in 2018, serious concerns exist surrounding the complexities of existing 3DIC technologies and their ability to scale. Thinned fragile substrates subjected to high peel or shear forces, heat, and burning, will likely require a new set of rules to manage a substrate that is 50% larger, thinner, and more costly.

B. DaeBond 3D™

Daetec has developed a new material and process, classified as disruptive to existing 3DIC practice. This technology, DaeBond 3D™, is based upon the use of a porous carrier (not perforated carrier). A porous carrier is made by applying a composite coating onto a carrier wafer. Device wafers are coated with a unique thermal resistant coating that achieves planarization. The device wafer is bonded to the porous carrier and processed through the customer's line. De-bonding occurs by chemistry using capillary driven penetration through the porous layer while the device wafer is supported onto the film frame, releasing the carrier within 15min. The batch driven process is conducted with a tape-safe chemistry in a simple wet bench tool offering low cost and throughput defined by the size of the cassette and tank.

C. Process

At the center of the DaeBond 3D™ technology is the formation of a porous coating onto the carrier.

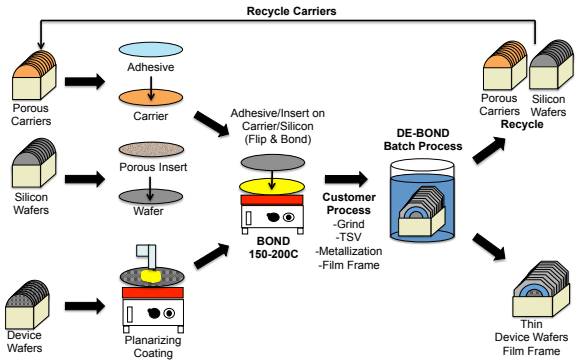

Fig. 3. DaeBond 3D™ technology process.

A range of coating practices is possible including spin, slit, or spray. Once completed, they are cycled through the customer's process a target of ten times.

D. Bonding & De-bonding

Device wafer topography is protected with the DaeBond 3D™ water-soluble planarizing coating. An edge bead removal step occurs to allow the adhesive layer to edge seal. The bonded wafer stack is now ready to support the customer process, including grinding, TSVs, metallization, and passivation (Fig. 4).

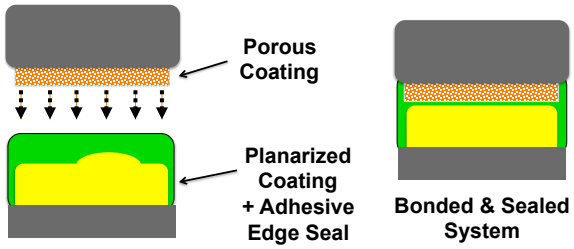

Fig. 4. DaeBond 3D™ bonding of the porous carrier to planarized device wafer.

Carrier de-bonding occurs by liquid penetration to break the edge seal and migrates swiftly through the porous coating until saturation causes a drop in adhesion whereby the carrier separates from the film frame. The film frames holding the thin device wafers proceed to tank 2 for cleans where DIW rinsing and drying occurs. At completion, the cassette contains taped film frames supporting thin wafers, ready for dicing (Fig. 5).

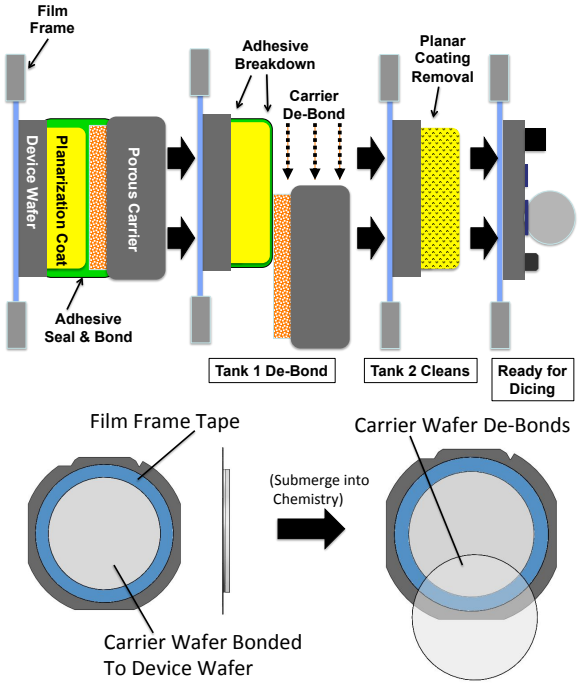

Fig. 5. De-Bond and cleans stepwise description (above) and release from tape (below).

E. Scaling to 450mm

Existing 3DIC processes are known to be complex, slow, and costly. As substrates get larger and thinner, these processes are projected to become more complex, costly, and suffer in yield. Assuming that 450mm is put online by 2017-18, substrate thicknesses will progress to reduce 50um or less.

The DaeBond 3D™ passive carrier de-bond system is considered to be scalable. Daetec has investigated fluid travel through the porous coating and other properties on varying substrate sizes. Results indicate minimal differences in debonding with substrate size. In other words, liquid penetration and travel varies little with substrate size. The parameters that control performance have little to do with substrate size, at least within the context of wafer sizes from 50-450mm.

II. Experimental

A. Materials

For process demonstration and testing, remanufactured silicon substrates at diameters of 100-200 mm (4-8") of known crystal orientation and thickness (1-0-0, ~525 µm; Wollemi Technical, Inc. Taiwan, www.wollemi.com.tw). Materials used include the following developmental products: a) porous coating (PCA-130608-001), b) planarization coating (PCA-130515-001), c) adhesive (PCA-130930-001-M20, and d) debond/cleans chemistry (SL-3300) [10]. Process chemistries include: TMAH (0.26N), isopropanol (IPA), n-methylpyrollidone (NMP), various dilute mineral acids, and sulfuric acid copper plating bath. Tape products for film frame applications include: Lintec

B. *Equipment*

Coatings are produced on a Brewer Science, Inc. CB-100 spin-coater, while spray and encapsulation uses custom tooling designed at Daetec. Metrology data is generated by a XP-1 stylus profiler, AFP-200 atomic force profiler, and a Xi-100 optical profiler [11]. Where applicable, equipment settings include a 5 mg stylus load, minimum 4 mm distance, and speed of 0.5 mm/sec. Bonding and debonding equipment is designed at Daetec for radiation and thermal cure.

III. RESULTS

A. *Properties Testing*

Daetec uses several monitors to control the quality of the porous coating. They include parameters as coating thickness, surface texture (roughness), and wick height (liquid travel distance). Methods have been developed to measure and control the material transport through the coating (Fig. 6).

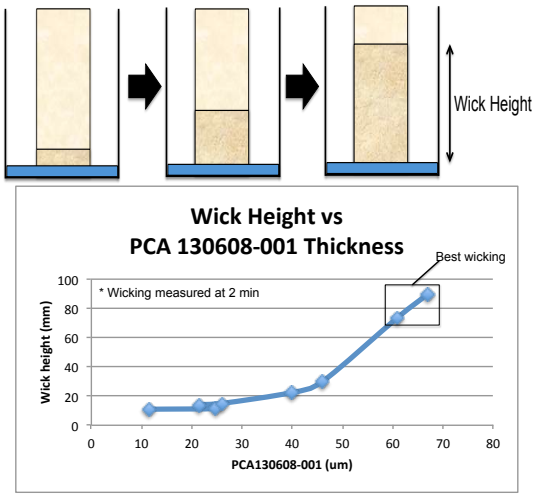

Fig. 6. Liquid travel through porous coating as wick height (above) and its relation to thickness (below).

Thermal outgas measurements are conducted by laboratory modified TGA methods on both the porous coating and adhesive. Exposure temperatures to 450C in a reducing environment have been confirmed (Fig. 7).

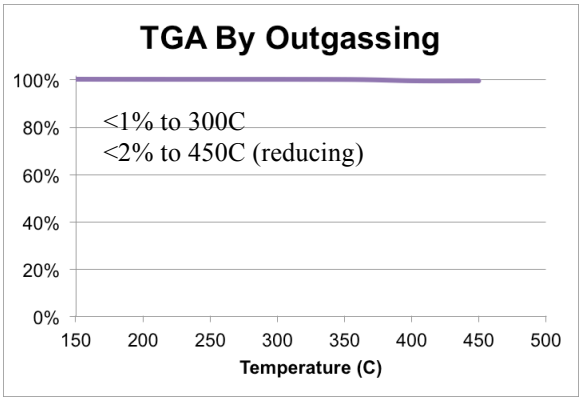

Fig. 7. Thermal outgas measurement of adhesive.

B. *Debond on Taped Film Frame*

Demonstration of film frame supported debond is conducted using a range of fixtures designed by Daetec. The wafer stack is affixed via the device wafer to a taped film frame. The bonded film frame is immersed into a liquid that initiates the debond process. The chemistry is safe for common tapes used in the industry.

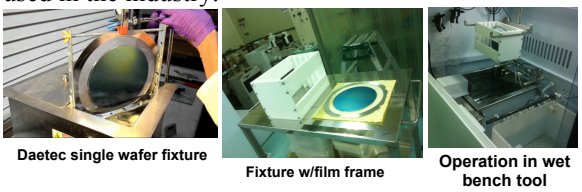

Fig. 8. Testing debond with mounted device wafers on film frames occur on single fixture, Teflon® multi-frame fixture and in a wet bench.

Extended time and temperature tests have been performed with several chemistries including SL-3300 to determine compatibility. Although some effects were observed, the majority survived, including several common acrylic tapes from leading suppliers (e.g. Furukawa, Lintec, and Nitto-Denko).

C. *Cost of Ownership*

There are many ways to assess the financial value of DaeBond 3D™, including cost of ownership (COO). Value is estimated as a ratio between two technologies, as COO_2 (DaeBond 3D™) and COO_1 (existing practice). Using calculations set forth in SEMI E35 [12], and setting tool costs of existing practice to be 2X while throughput to be 20% of DaeBond 3D™, the cost to implement DaeBond 3D™ is shown to be 10% of an existing technology that uses thermal, peel, or radiation (laser) release. Calculation of comparative COO is given in Fig. 9 while expected costs and throughput changes in each respective technology with scaling to HVM is shown in Table 2.

$$\frac{COO_2}{COO_1} = \frac{\text{DaeBond 3D}}{\text{Existing Technology}}$$

$$\frac{COO_2}{COO_1} = \frac{F\$_2 \times T_1}{F\$_1 \times T_2} = \frac{F\$_2}{F\$_1 \times 5}$$

$$\frac{COO_2}{COO_1} = 10\%$$

Fig. 9. Comparative COO calculations (example #1).

Table 2. Comparative COO calculations (cost ratio) as each technology move towards HVM.

#	DaeBond 3D Tool ($m)	Existing Tech Tool ($m)	DaeBond 3D Throughput (wph)	Existing Tech Throughput (wph)	Cost Ratio (%)
1	0.75	1.5	100	20	10.0%
2	0.5	1.5	100	20	6.7%
3	0.5	8	100	30	1.9%
4	0.5	8	400	30	0.5%

IV. Discussion

Many adhesive platforms exist to support 3DIC processing towards HVM. For reasons of poor throughput, low yield, and high cost, these technologies represent one of the greatest challenges for the industry to overcome. DaeBond 3D™ is a new technology with many benefits (Table 3).

Table 3. Benefits of DaeBond 3D™.

Benefits	Explanation
High Yield	Planarized layer – protection Continued support – film frame Passive debond w/porous coat
Adhesive	Chemical & thermal resistant Soluble in tape-safe chemistry
Low-cost tool	Common wet-bench
High Throughput	100wph baseline (1 cassette)
Film frame	Tape-safe compatibility
Carrier recycle	10 cycles before re-apply
Scalable	Penetration/saturation is non-linear relative to substrate size
Green process	Tape-safe de-bond, DIW cleans

Measured properties of the porous coating are presented here to help the reader understand the performance of this new technology. Properties of wicking on a small scale translate to liquid penetration and debond of wafers that scale in size.

V. Conclusions

This paper introduces a new technology based upon the design and use of a porous coating. DaeBond 3D™ offers many benefits to drive down the COO to a minimum of 10% the comparable cost of implementing an existing technology. As more tuning and emphasis towards increased throughput occurs, this value will continue to drop.

Acknowledgment

The authors would like to thank the staff at Daetec for their support in making this work possible.

References

[1] U.S. Patent No. 7,678,861, J. Moore et.al.
[2] U.S. Patent Nos. 6,869,894, 7,098,152, and 7,232,770, J. Moore, et.al.
[3] U.S. Patent No. WO 2010/107851 A2, J. Moore, et.al.
[4] Semicon-West, San Francisco, CA, SEMI/panel discussion, July, 2013. (http://www.semiconwest.org/sites/semiconwest.org/files/docs/SW.ShowDaily13.Day3_.FP_.low_.pdf).
[5] C. Orlando, T. Goodrich, and E. Gosselin, Backside Mounting Procedures for Semiconductor Wafer Processing, *Proceedings for GaAs MANTECH,* 2001, pp. 189-191.
[6] J.Moore, Materials and Conditions Used to Optimize Thinning, Processing, and Dismounting GaAs Wafers, *SEMICON-WEST Technical Symposium (STS): Innov. Semi. Mftg.*, July 2001, pp. 339-348.
[7] I. Blech and D. Dang, "Silicon Wafer Deformation After Backside Grinding, *Solid State Technology,* August 1994, pp. 74-76.
[8] C. McHatton and C. Gumbert, Eliminating Backgrind Defects With Wet Chemical Etching, *Solid State Technology,* November 1998, pp. 85-90.
[9] Semicon-West, San Francisco, CA, SEMI/Gartner marketing symposia, July, 2013. (http://www.semiconwest.org/sites/semiconwest.org/files/docs/SW.ShowDaily13.Day1_.FP_.low_.pdf
[10] Spin coatings, adhesives, encapsulants, cleaners, equipment, and processing designs utilizing a wide range of cure approaches including evaporative, photo, and thermal are from Daetec, LLC, www.daetec.com.
[11] Series XP, AFP, and Xi, are contact and non-contact profilometers as produced by Ambios Technology, Inc., www.ambiostech.com.
[12] Guide to Calculate Cost of Ownership Metrics for Semiconductor Equipment, SEMI Standard E35-037, www.semi.org.