Temporary Bonding of Wafers, Displays, and Components

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Contents

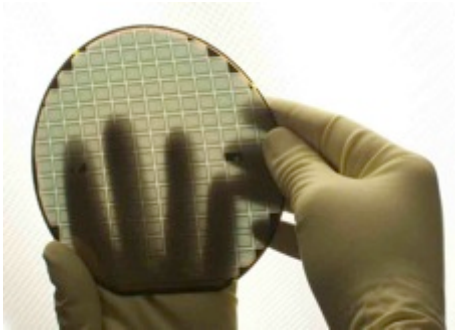
1. Adhesives & Substrates
2. Wafers
3. Displays
4. Devices

Electronics Everywhere

- Auto & Medical - diagnostics
- Aircraft - entertainment
- Communication
- IOT - surveillance & traffic

Thin Substrate Market Drivers

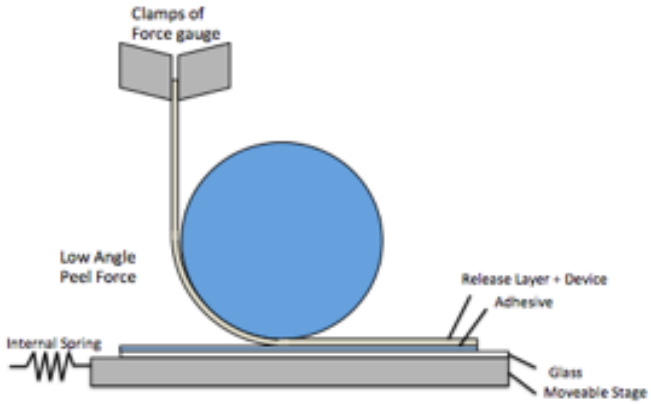
- Electronics trending thinner
- Smart phones, tablets, etc.
- Diced chips are stacked
- Stacked chips used in all functional devices
- Extremely fragile
- Requires a temporary support

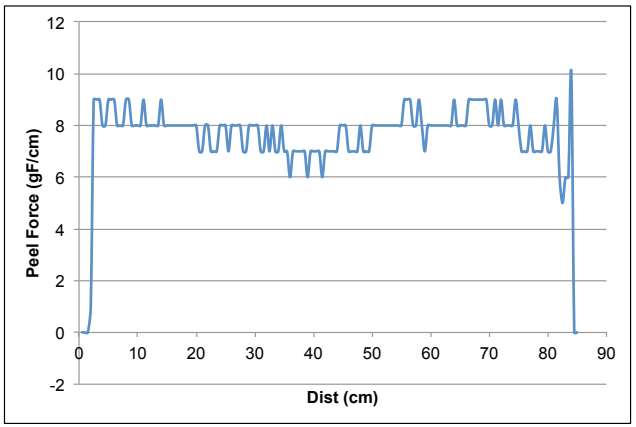


1. Adhesives & Substrates

- Matched to substrate needs
- Surface energy (lower vs substrate)
- Thermal & chemical resistant
- Low outgas (high Tg or barrier)
- Inert & easy to clean

World of Temporary Bonding

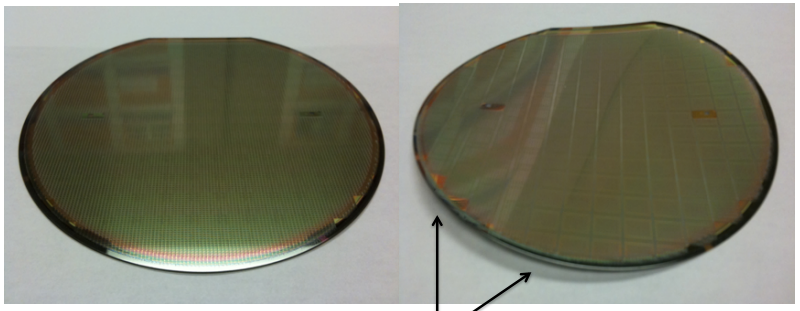




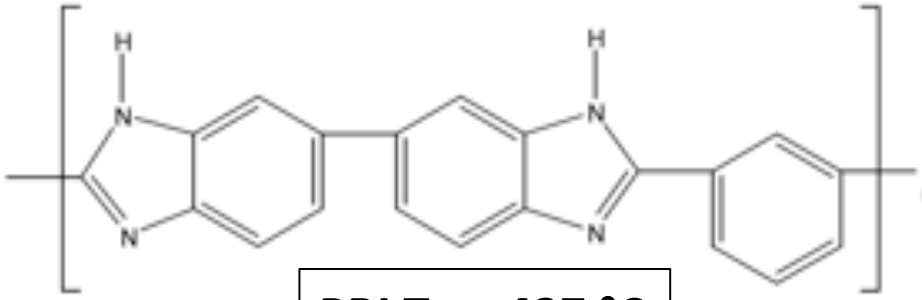
Work Unit	Market	DaeCoat™	Method
Organic Film	OLED, flexible displays	350	Cure on carrier, bond w/pressure
Organic Film (cast)		310	Cure on carrier, cast & cure liquid
Thin glass	TFT LCD	350	Cure on carrier, bond w/pressure
Foil	OLED, flexible displays	350	Cure on carrier, bond w/pressure
Wafer	3DIC	350, 615, 620	Planarize wafer w/550, cure on carrier, bond w/pressure
Die (chip)		350	Cure on carrier, bond w/pressure

Substrate Types

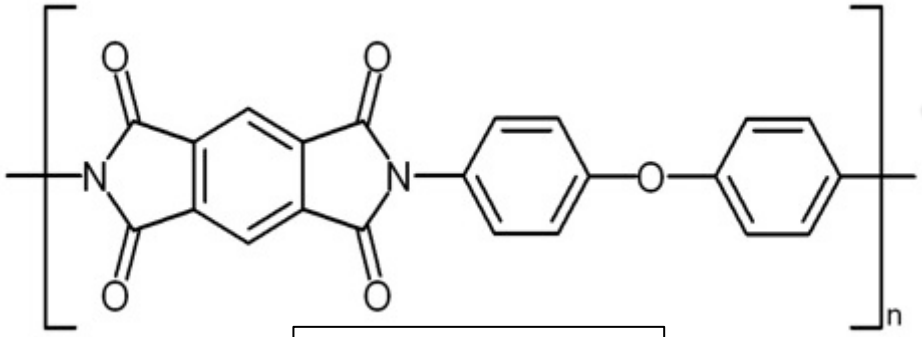
- Rigid: silicon, quartz, glass, sapphire
- Flexible: PI, PEN, Arylite, PPS, PET, epoxy
- Ideal characteristics: CTE match, low TTV
- Other qualities: transparency, tensile, barrier
- Dimensions: application specific



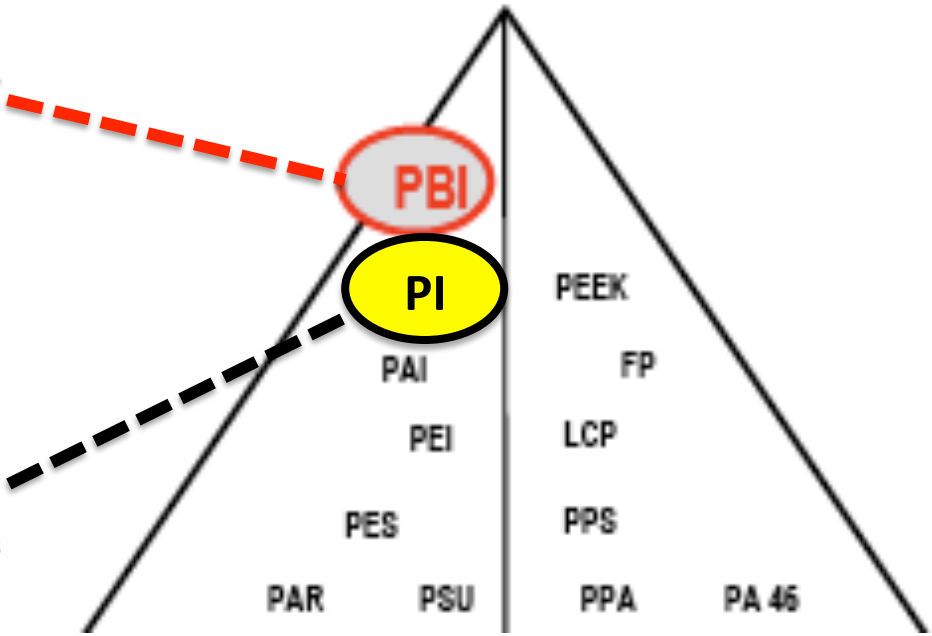
Engineering Polymers



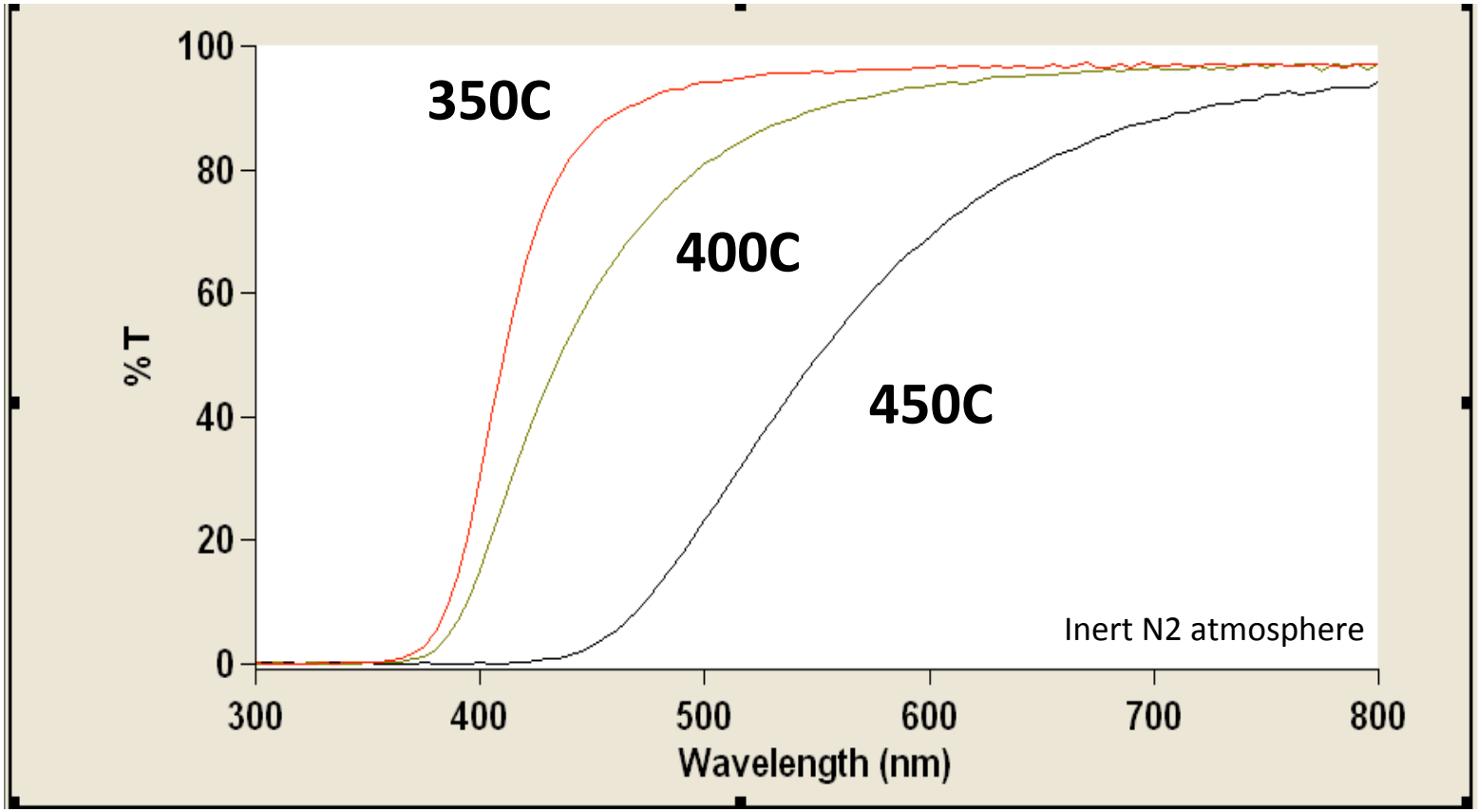
PBI Tg = 427 °C



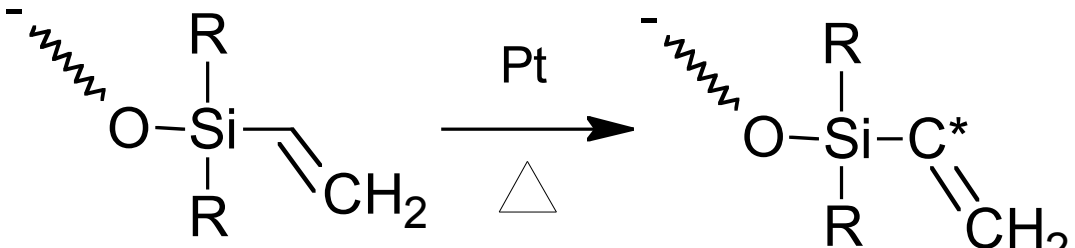
PI Tg = 370 °C



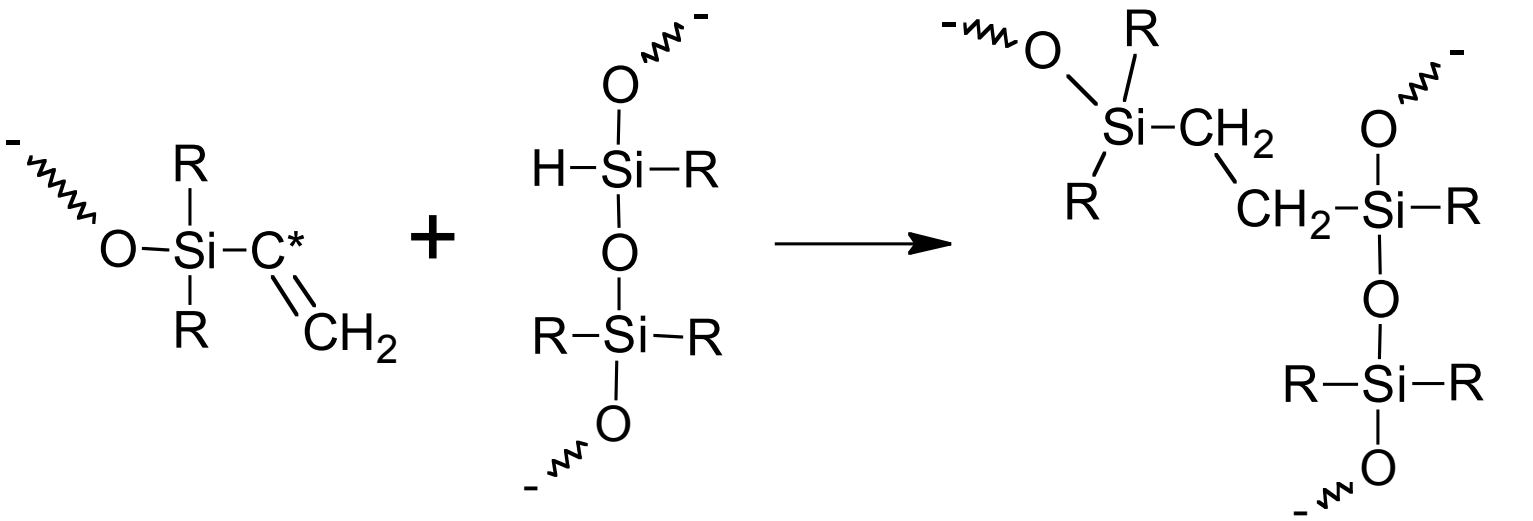
Typical PI Transparency Thermal Trend



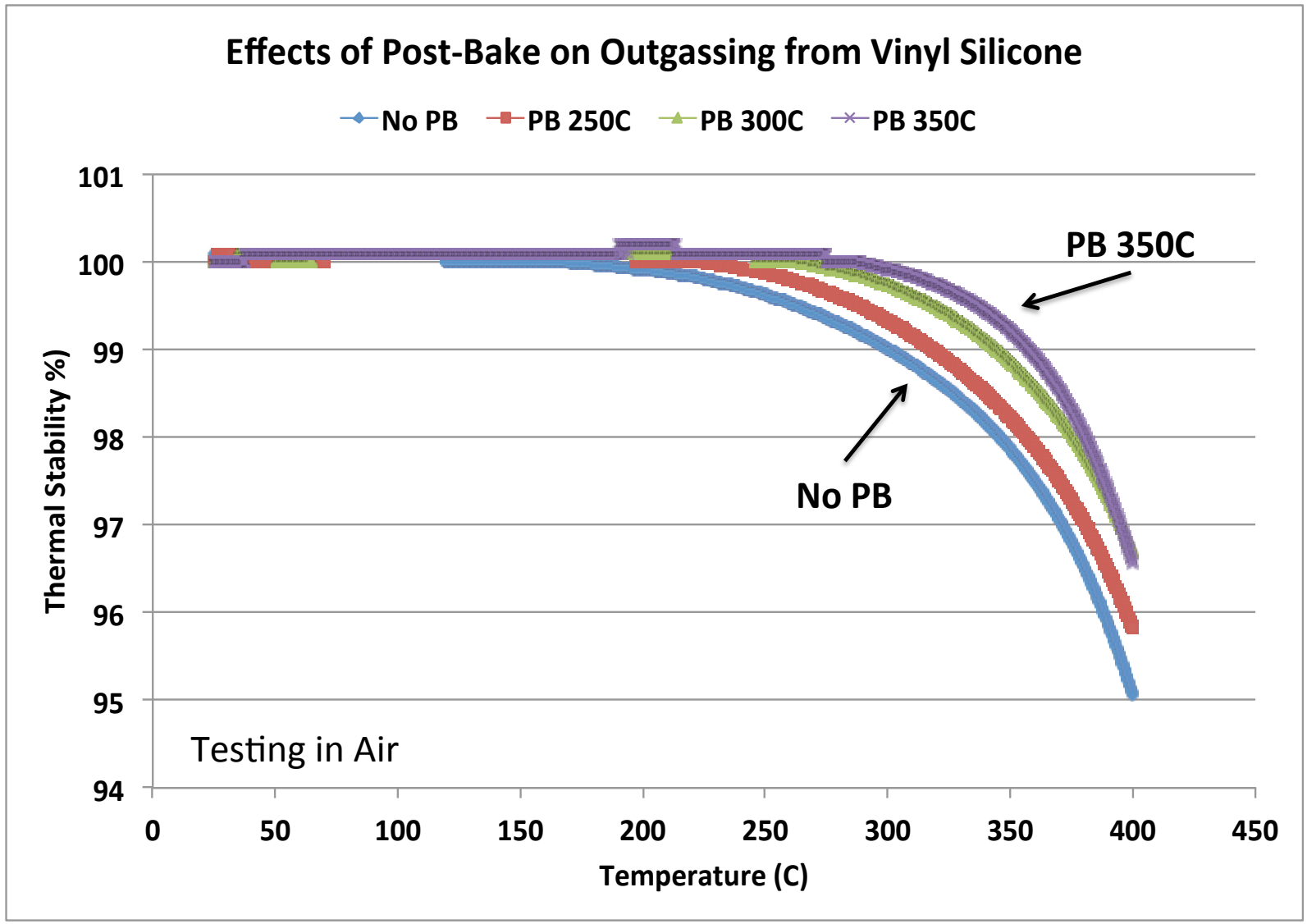
Silicone Thermoset (catalytic)



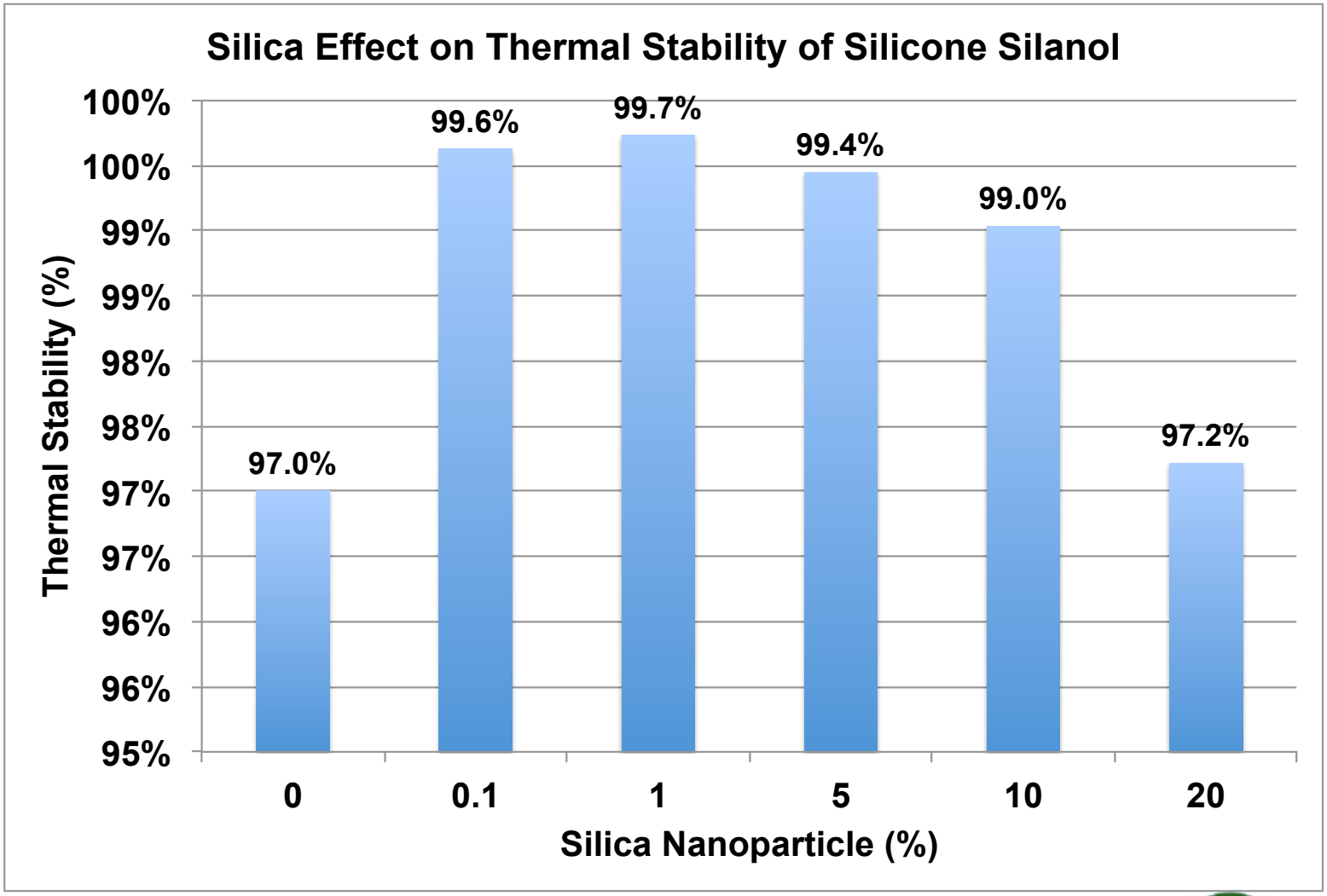
Resin monomer (MW & shape) **Free-Radical**



Activator monomer (MW & shape) **Silicone Polymer**

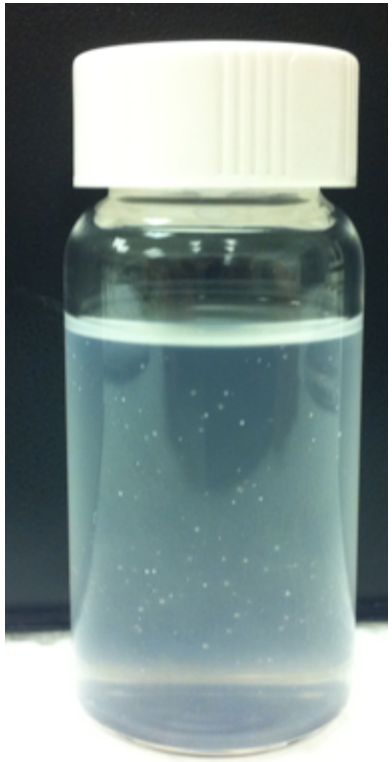

Effects of Post-Bake on Outgassing from Vinyl Silicone
No PB
PB 250C
PB 300C
PB 350C
Thermal Stability %)
101
100
99
98
97
96
95
94
0
50
100
150
200
250
300
350
400
450
Temperature (C)
PB 350C
No PB
Testing in Air

Silicone 400C Thermal Resistance



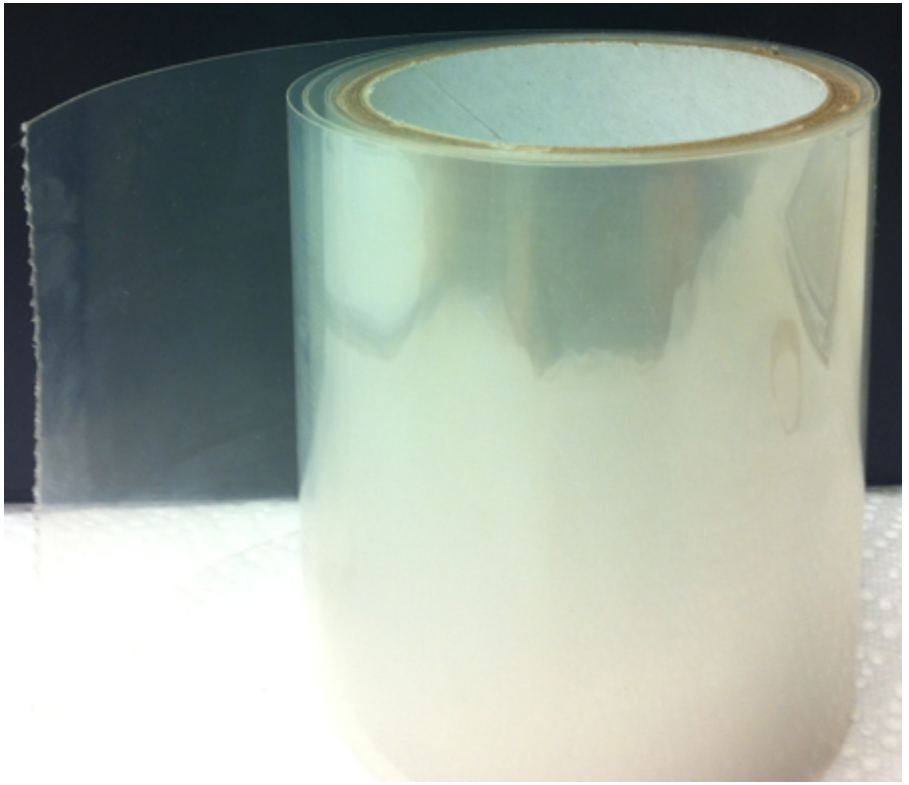
Adhesive in Several Forms

Liquid

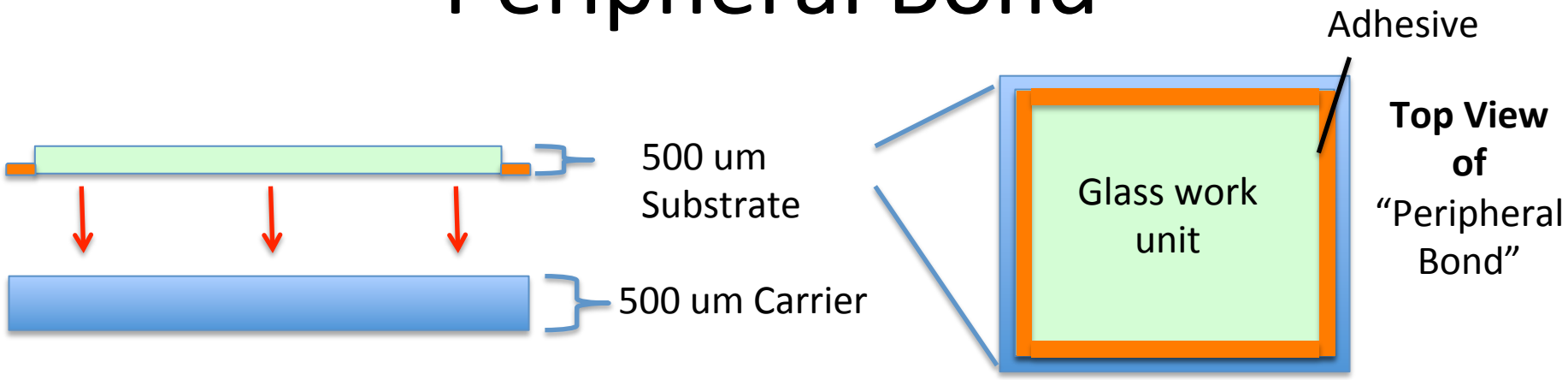


Gel

Film

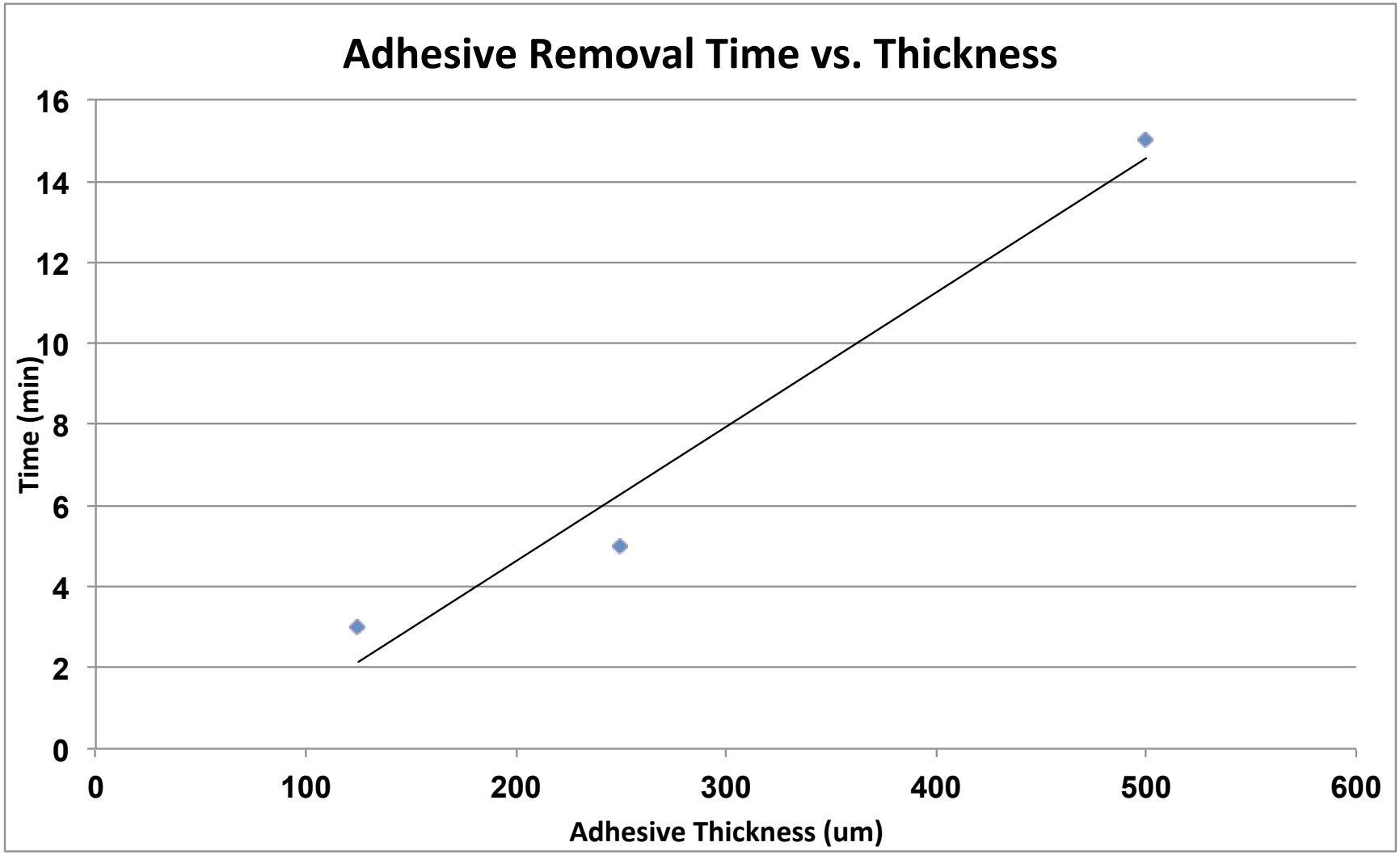


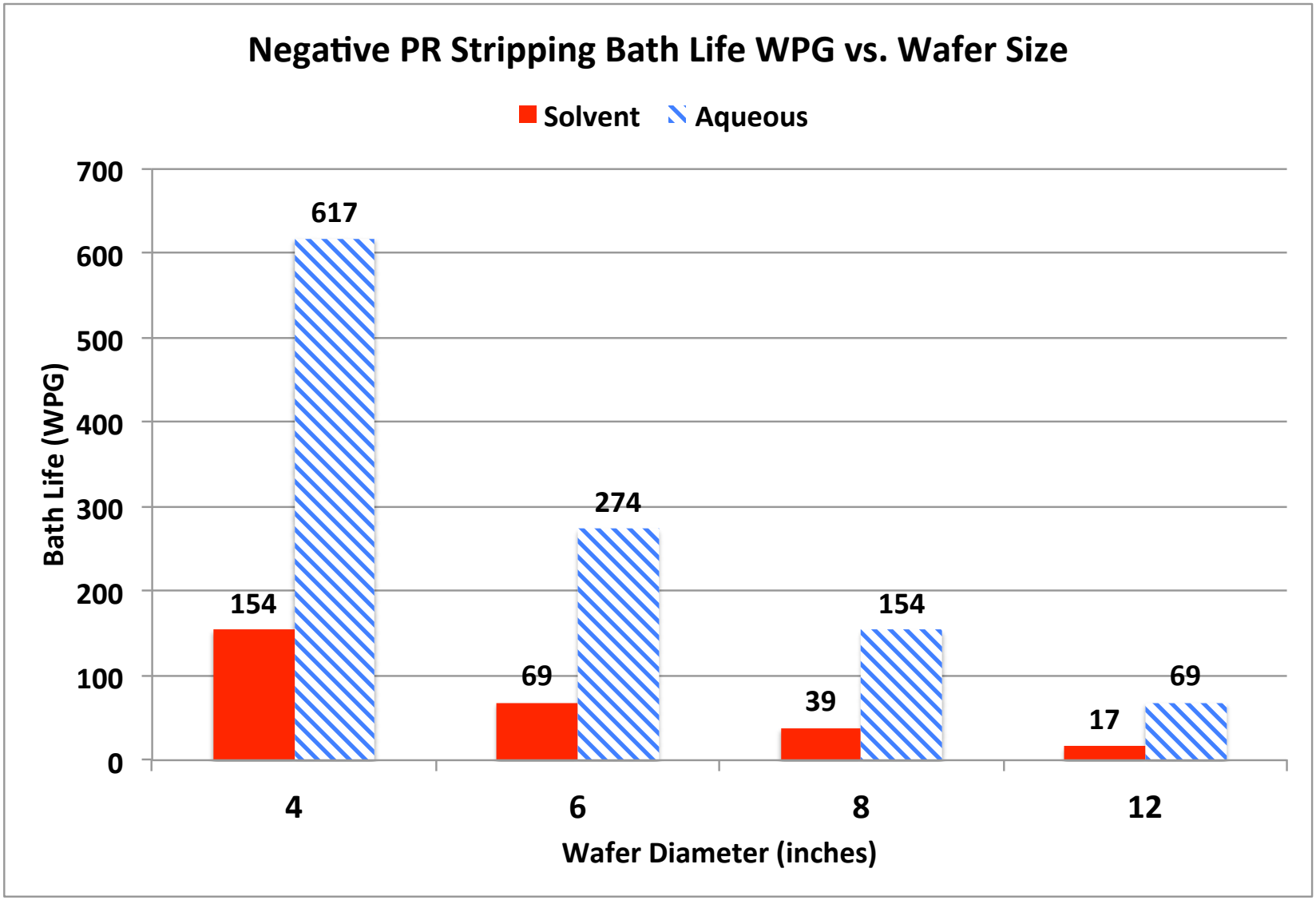
Peripheral Bond



- The adhesive may be applied on the edges of the carrier – known as *peripheral bond*
- Thin substrate is bonded onto carrier
- Adhesive undergoes heat cure

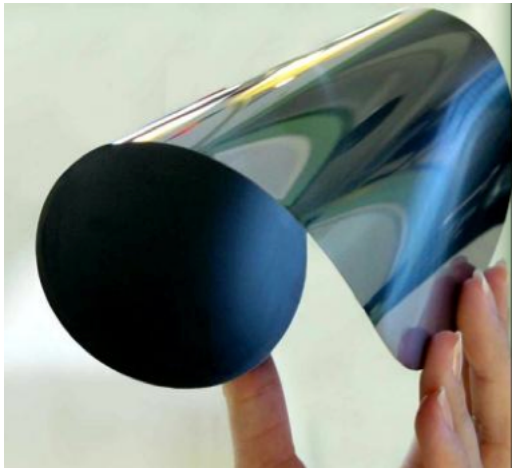
✪ 7.periph. bond

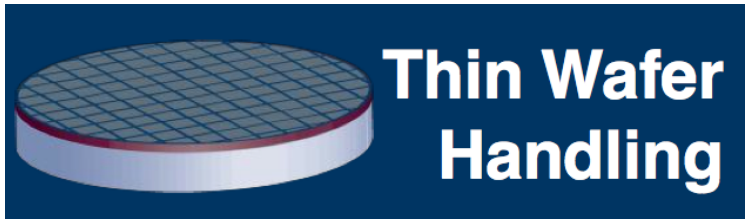

Adhesive Removal Time vs. Thickness
Time (min)
16
14
12
10
8
6
4
2
0
0
100
200
300
400
500
600
Adhesive Thickness (um)


Negative PR Stripping Bath Life WPG vs. Wafer Size
Solvent
Aqueous
Bath Life (WPG)
700
600
500
400
300
200
100
0
617
274
154
154
69
69
39
17
4
6
8
12
Wafer Diameter (inches)

2. Wafers

- Wafers thinned to <100um
- Carriers are required
- Debonding generates problems, can be a bottleneck, high cost, and source of yield loss





Creating a Process

- Device Wafer: planarized, edge trim (thickness)
- Carrier: CTE closely matched, TTV <2um
- Adhesive: thermal & chemical resistant, thin & uniform, if thick (high modulus)
- Bond: low temp (CTE)
- Debond: passive & cleans complete

Planarization Coating

Wafer with Topography (planarize >100um)

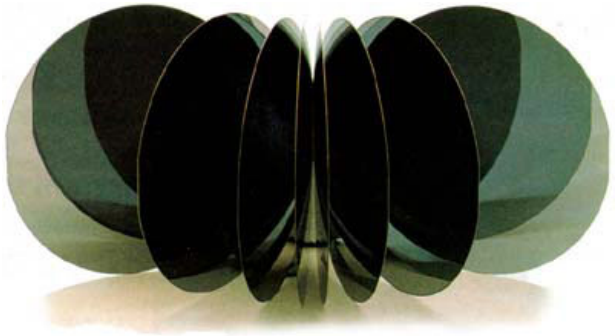
Planarization Coating

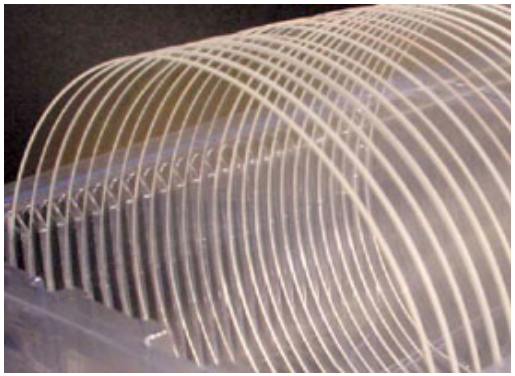
Planarized Surface

DaeCoat™ 515 – DIW washable

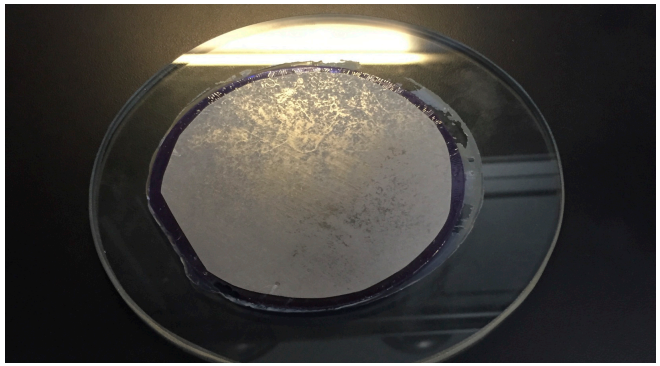
Carriers

- Silicon
- Glass
- Sapphire
- Tape

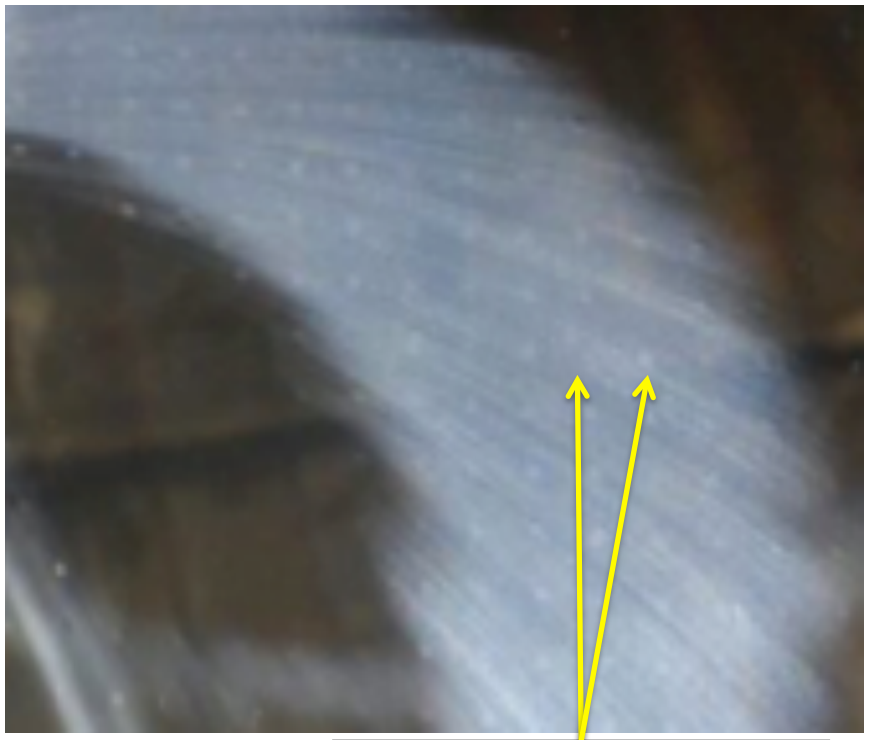




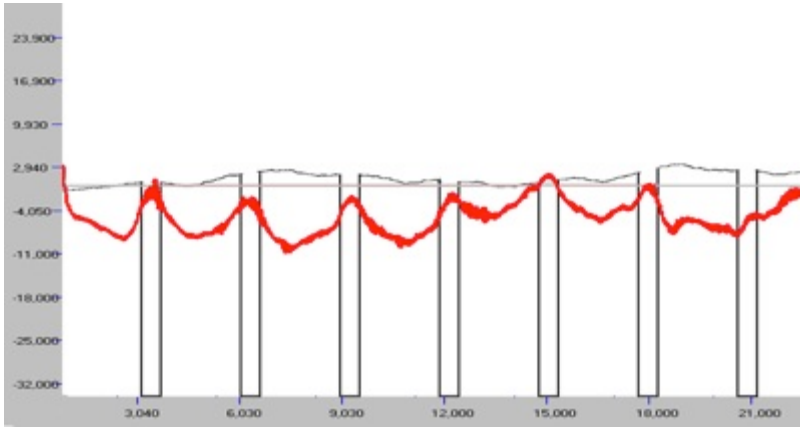
Porous Carriers



Perforated Glass, 50 µm



Divots from glass pores



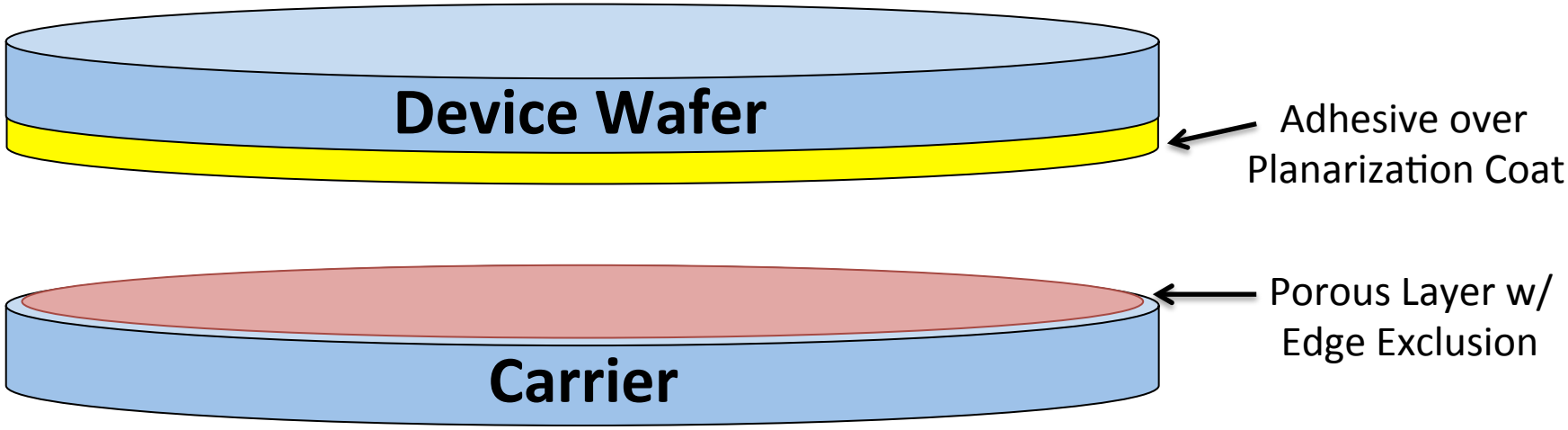
Black: Surface Scan of Perforated carrier
Red: Surface Scan of ground wafer with perforated carrier

Surface Scan shows the divots from glass pores

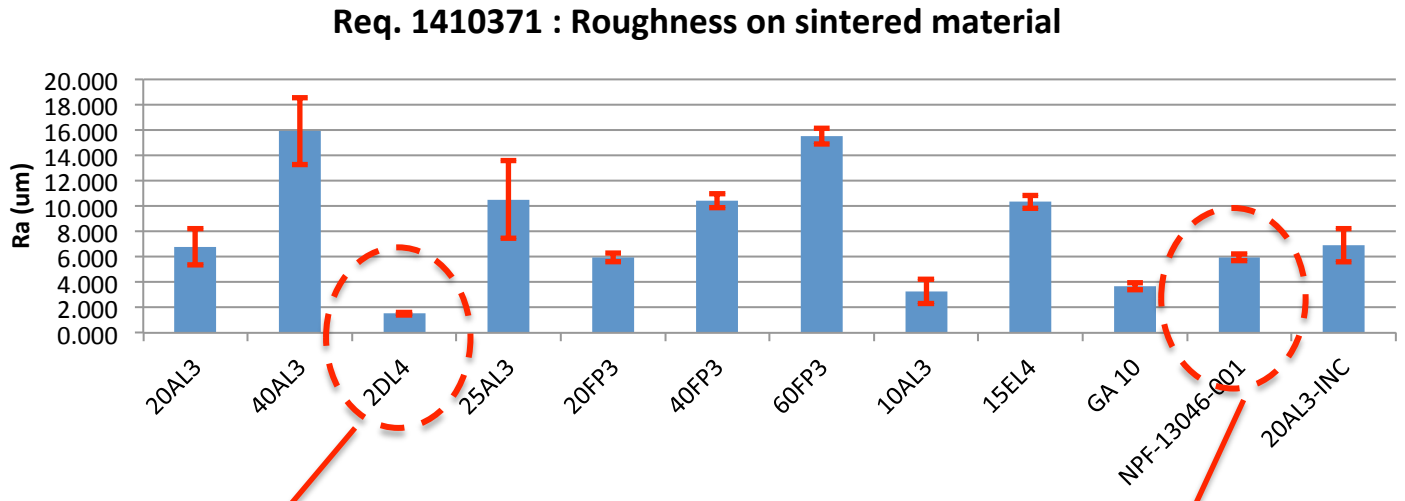
Porous Carrier

Benefits

- Thermal & chemical resistant
- Simple bond, high adhesion
- Accepts many adhesive types
- Passive debond (chemical diffusion)
- Device wafer on film frame
- Recycle >10X



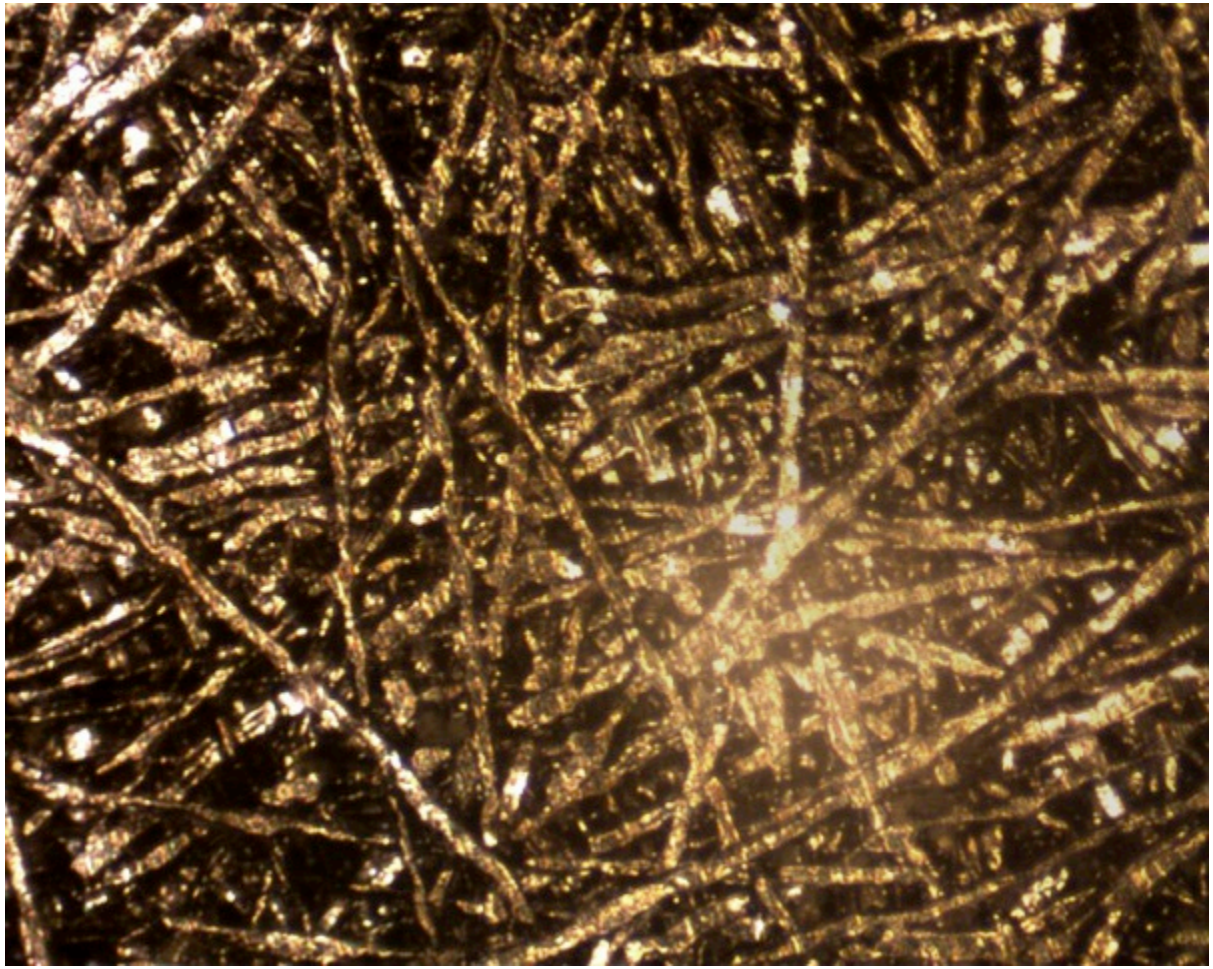
Porous Metal Carrier Media



Smooth (lowest Ra) in the product line

- Mid-range smooth product
- Ti is only non-ferrous product acceptable by fabs

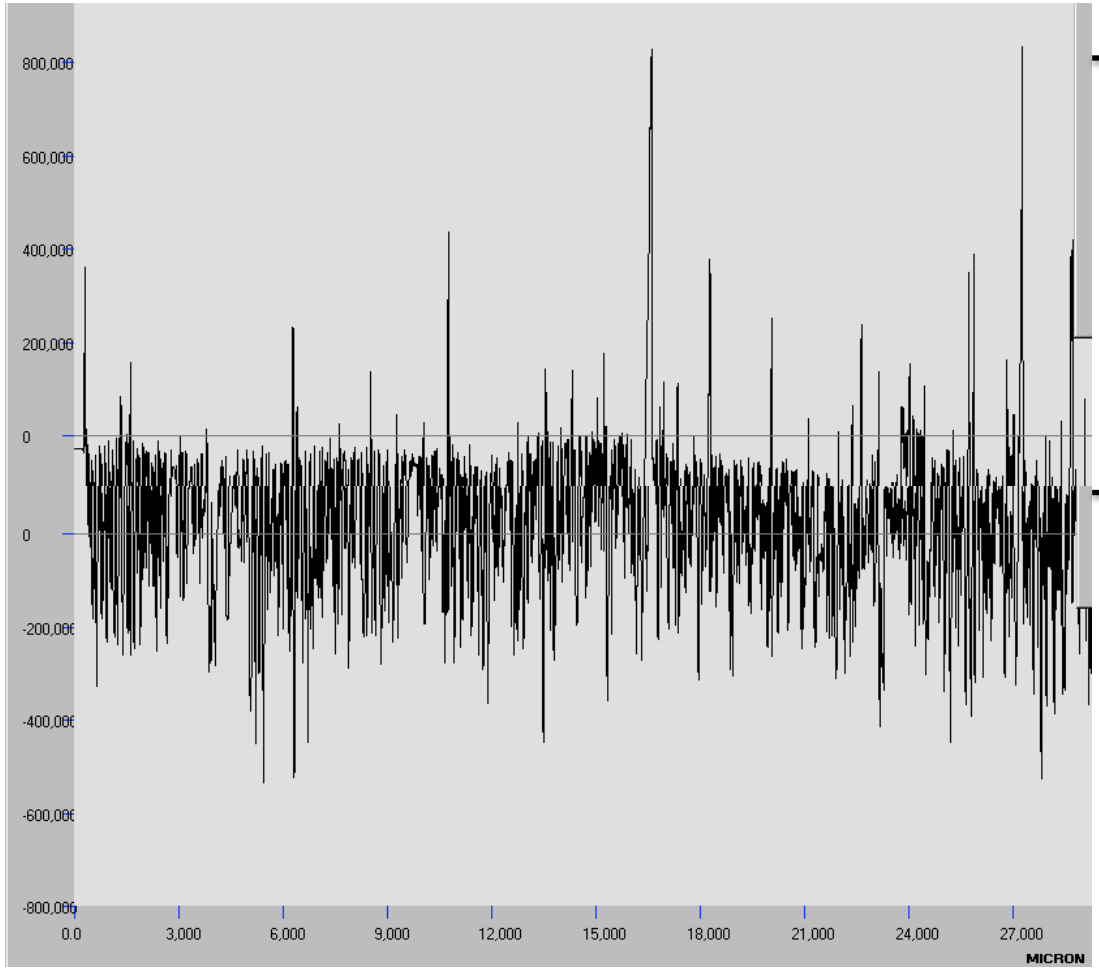
Ti Porous Metal (Microscopic)



Surface Scan of Porous Ti

Ti has stray wires reaching <80µm

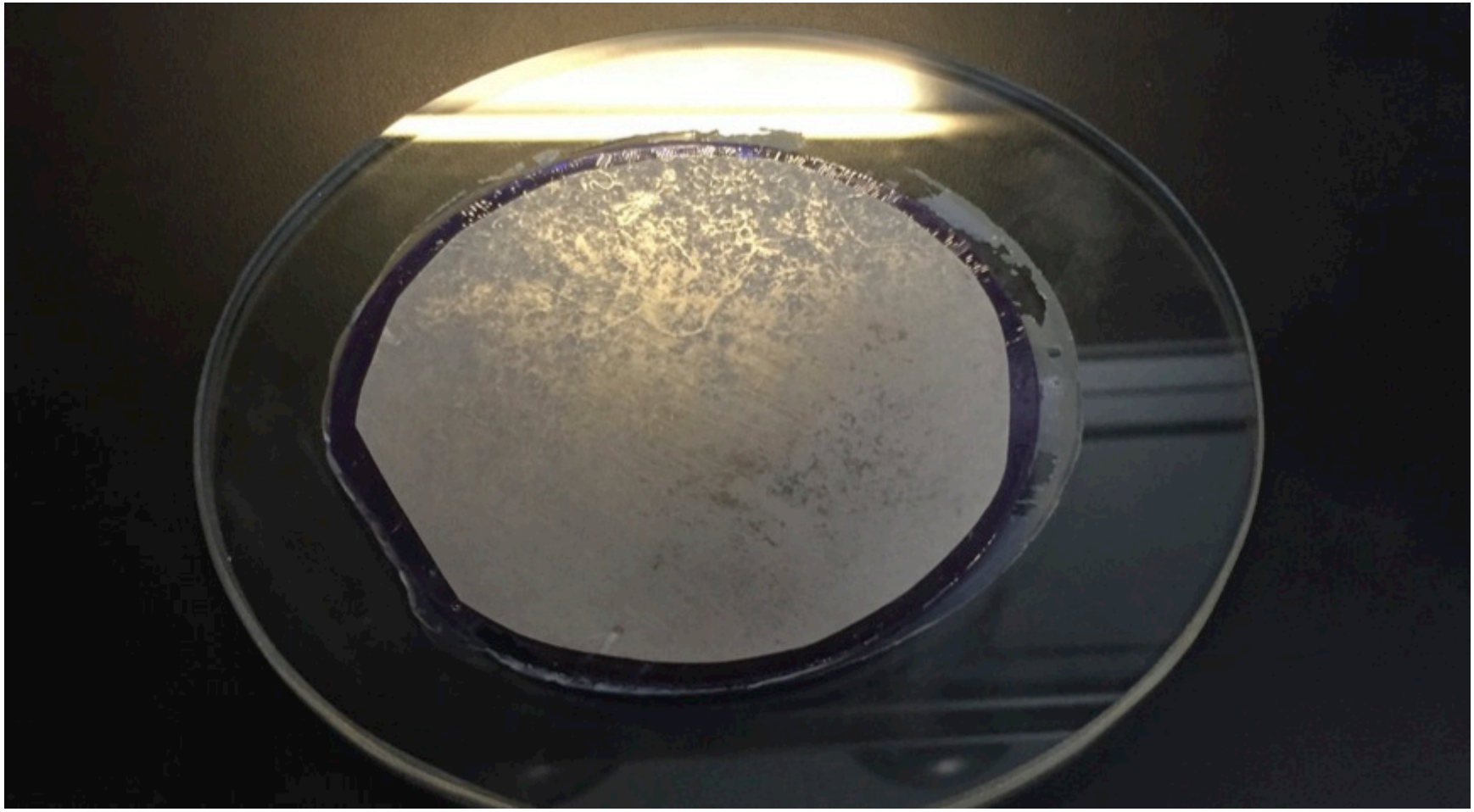
Angstrom



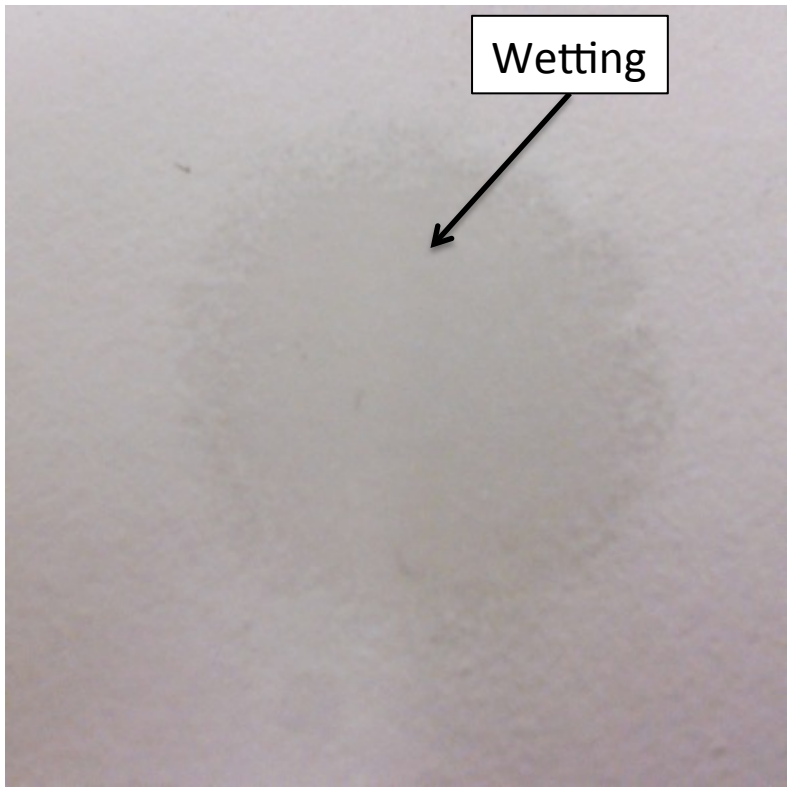
Micron

Porous Metal Carrier

Polishing to TTV



Surface Treatment



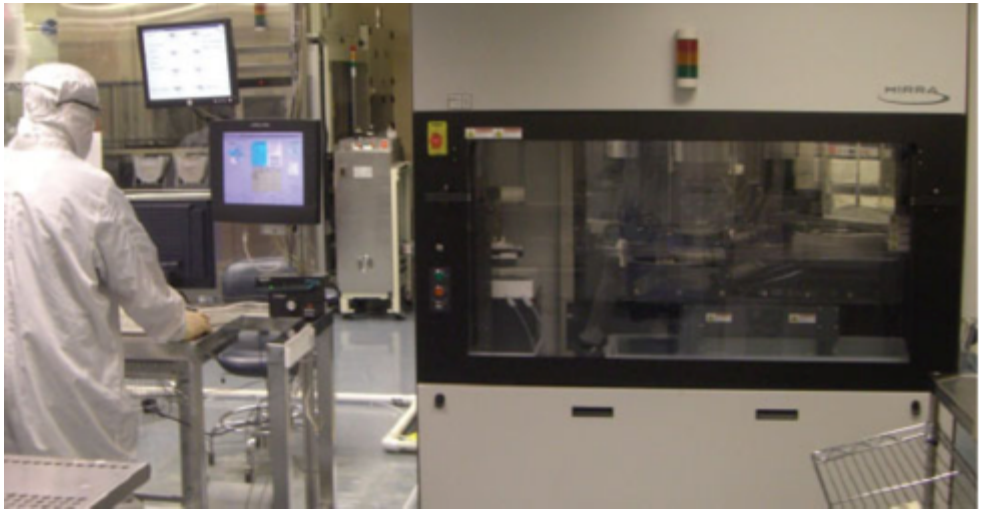
Without Exclusion Layer

With Exclusion Layer

Wafer Grinding & Testing

Strausbaugh

- Use a local grind/polish firm (Arizona, USA)
- Equipment is consistent with that used in fabs
- Scientists have a high degree of experience



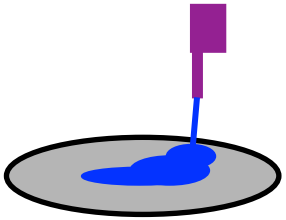
Process

Commercial Technologies

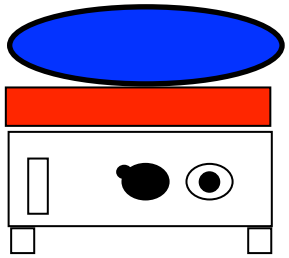
	BSI (Zonebond)	3M	TMAT	Dupont	Dow Corning	DOW
Bond type	Thermoplastic	Thermoset	Thermoset	Thermoplastic	Thermoset	Thermoplastic
Debond type	Slide + CRT /Peel	Laser, Peel	Peel	Laser + CRT	Peel	Peel
Tooling	Thermoslide/Peel tool	Laser tool, Peel tool	Peel tool	Laser tool, Peel tool	Peel tool	Peel tool
Post processing	Cleans, tape isolation	Cleans, Tape isolation	Cleans, Tape isolation	Cleans, Tape isolation	Cleans, tape isolation	Cleans, tape isolation
Temperature	≤250°C	≤250°C	≤300°C	≤450°C	≤300°C	>300°C
Additional challenges	Cleans	Transparent carriers	None	Transparent carriers Lengthy curing cycle	Cleans	None
Key benefits	RT Debond	RT Debond	RT Debond	High temp processing, RT debond	RT Debond	High temp processing, RT debond

Process Flow – Porous Carrier

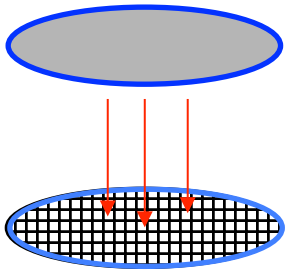
Silicon Substrate



Spin Coat Adhesive
Apply Adhesive to silicon device



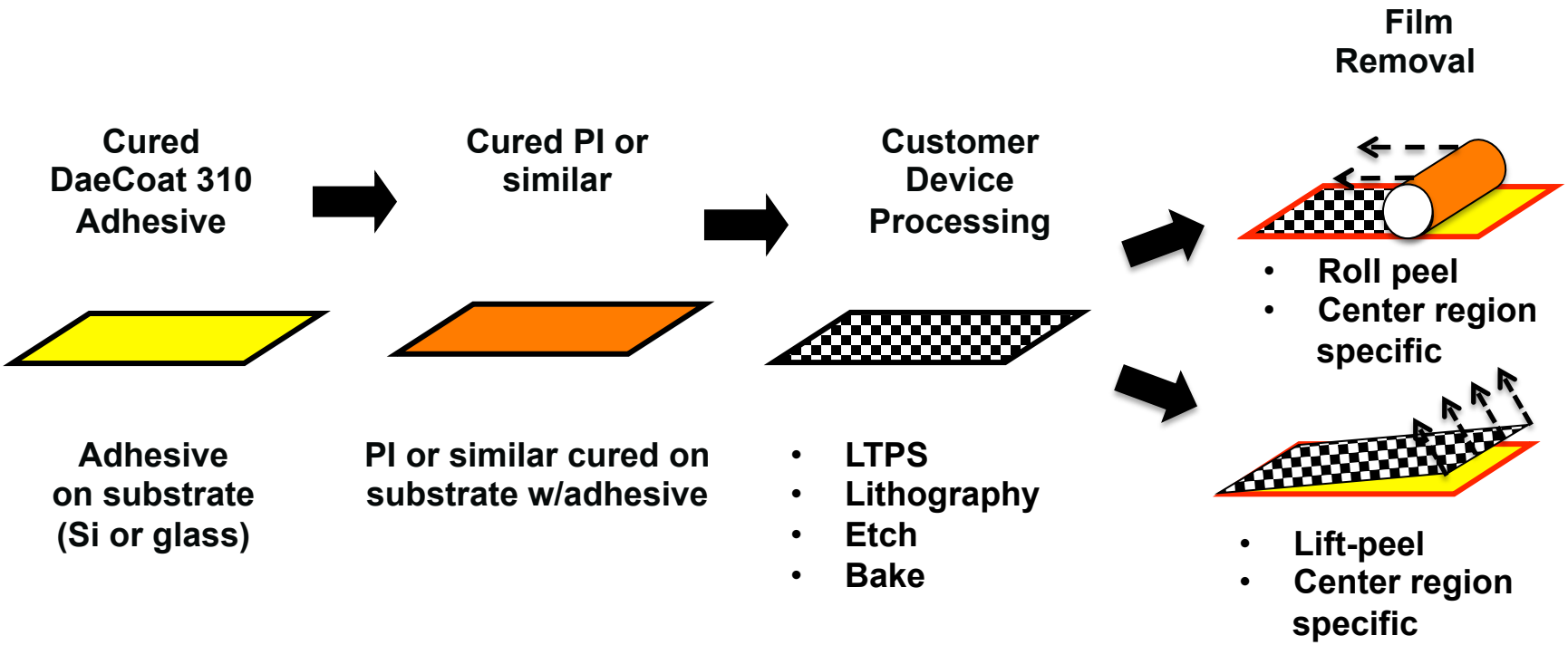
Cure Adhesive
Prepare for Dry-bond



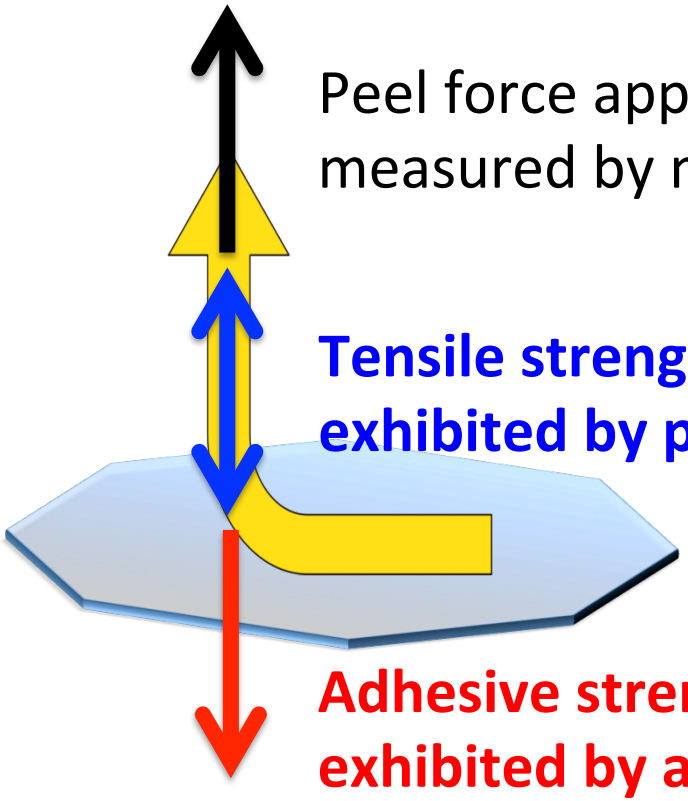
Dry-Bond
25-30C, 5min in Bonder
(Pressure ~15psi)

Subsequent Steps
Thin
Debond

3. Displays


Cured DaeCoat 310 Adhesive
Cured PI or similar
Customer Device Processing
Film Removal
Adhesive on substrate (Si or glass)
PI or similar cured on substrate w/adhesive
• LTPS
• Lithography
• Etch
• Bake
• Roll peel
• Center region specific
• Lift-peel
• Center region specific

Discussion



Peel force applied by and measured by meter

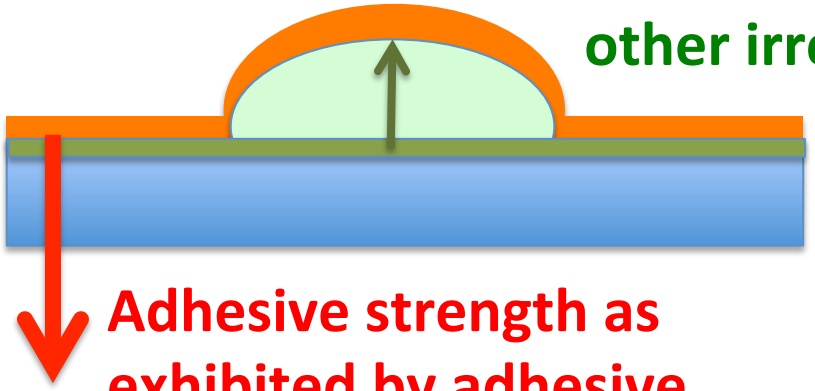
Tensile strength as exhibited by polymer

Adhesive strength as exhibited by adhesive layer

Model of thin substrate peeling with adhesive layer, minimizing bubble formation

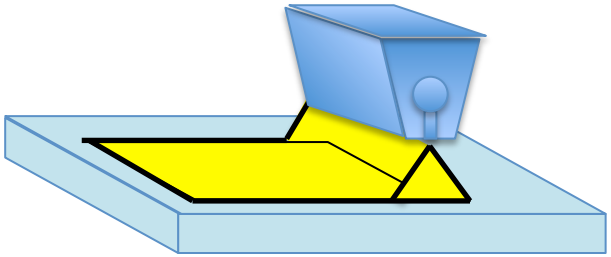
Bubble Model

Bubble forms when force of irregularity > adhesive

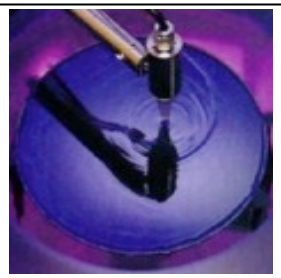


Adhesive: DaeCoat™ 310

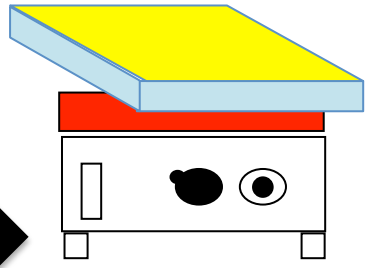
Mix A,B and C
Filter (0.2micron)



Slit Coating:
1. Adjust Gap height (<1 μm)
2. Apply



Spin Coating:
1. Dispense
2. 500rpm (60sec)



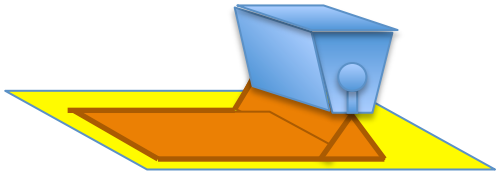
(Hot Plate)

Curing
1. 150°C (5min)
2. 250°C (15min)

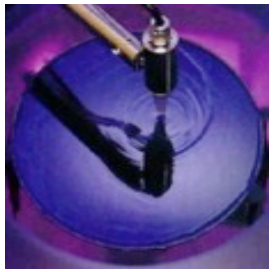
PI or Similar Coating

Daetec's Polyimide: DaeCoat™ 210

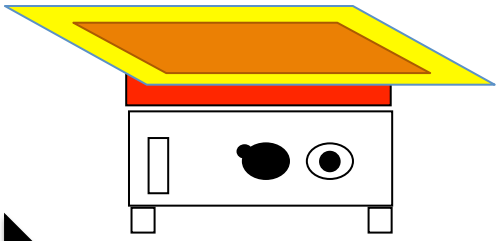
Cured
DaeCoat™ 310



Slit Coating:
1. Adjust Gap height (10-40μm)
2. Apply



Spin Coating:
1. Dispense
2. 1000-2000rpm (60sec)

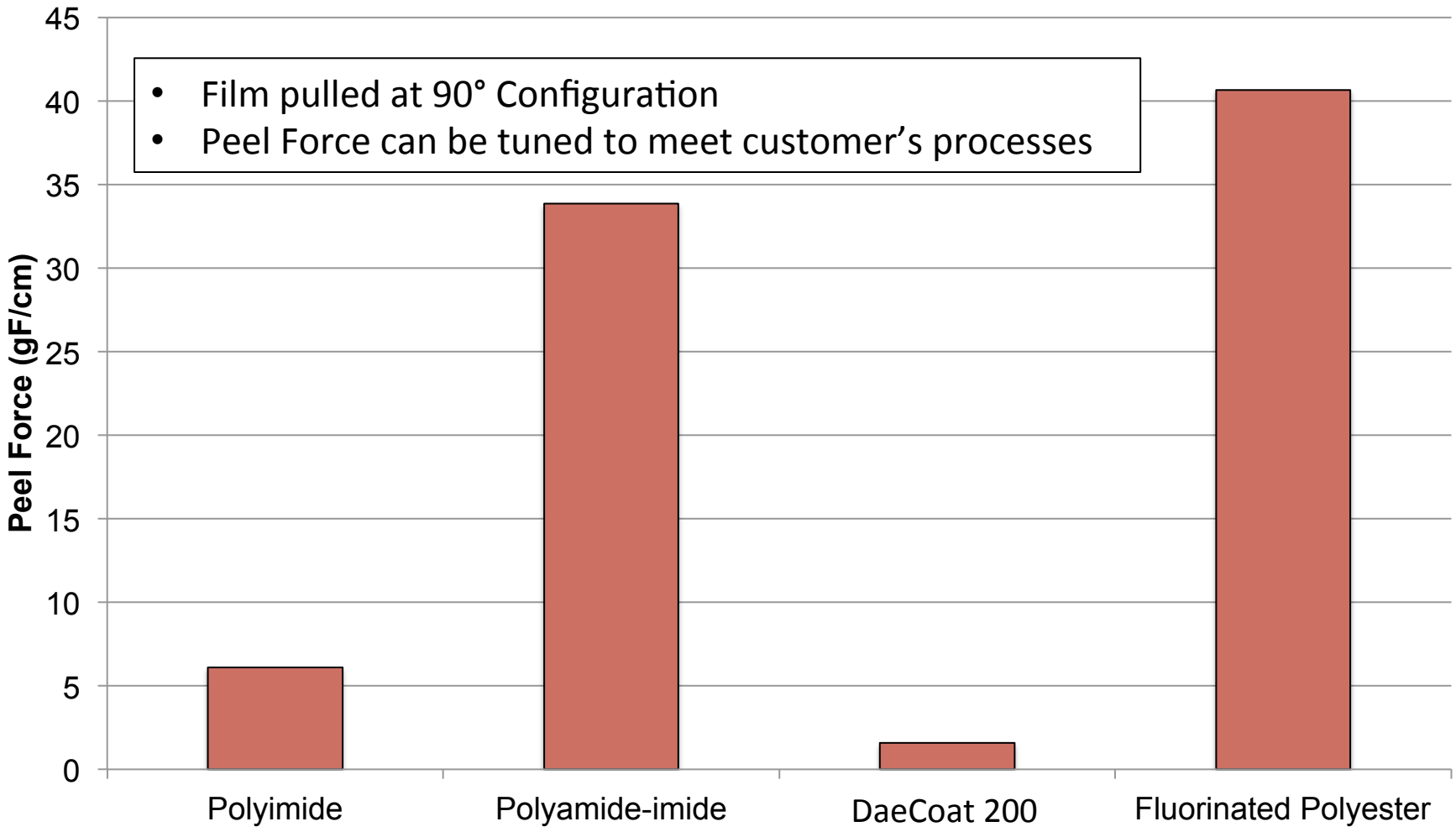


(Hot Plate)

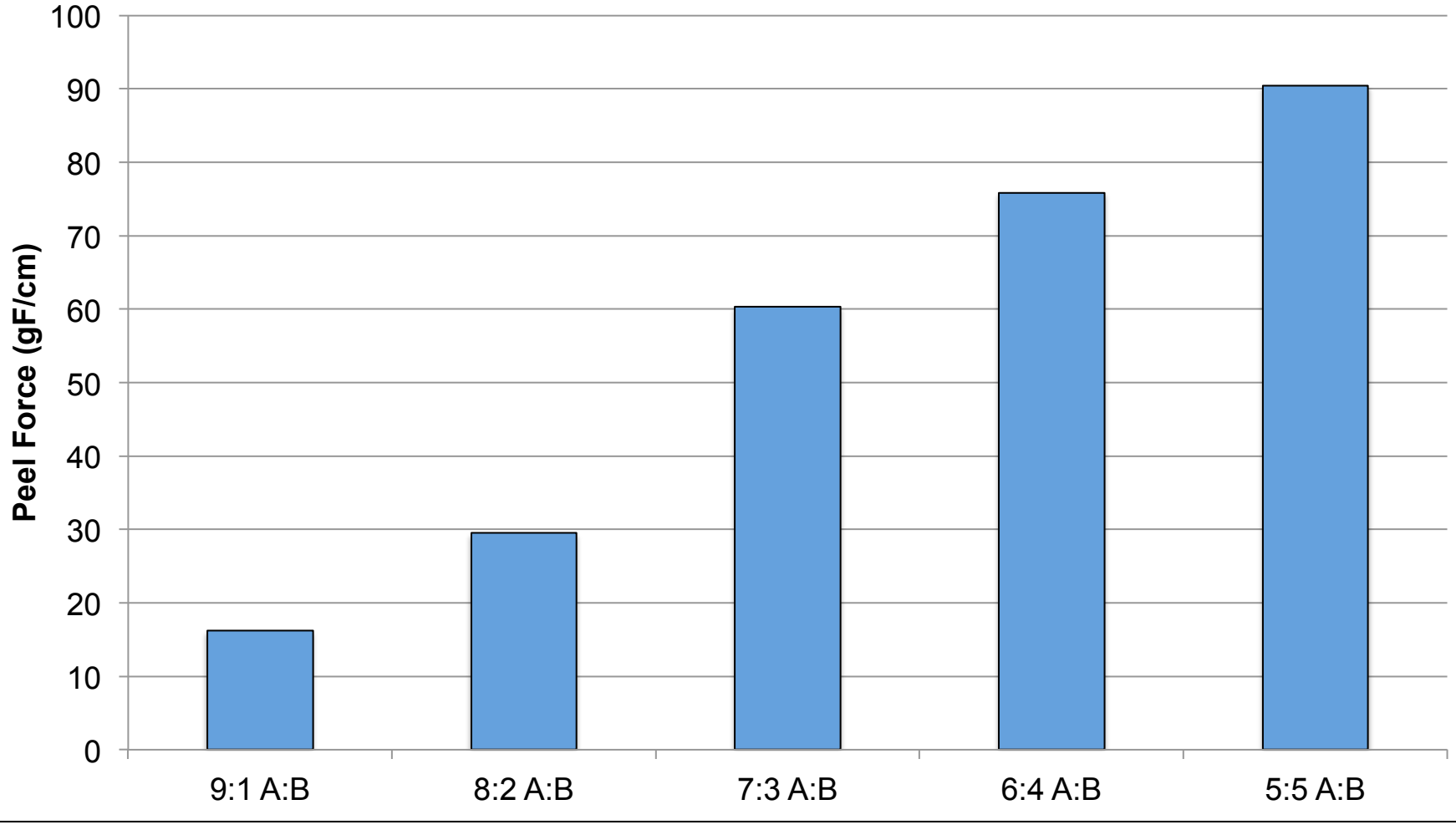
Curing
1. 150°C (5min)
2. 250°C (15min)
3. 350°C (10min)

Peel Force of Liquid Cast Materials

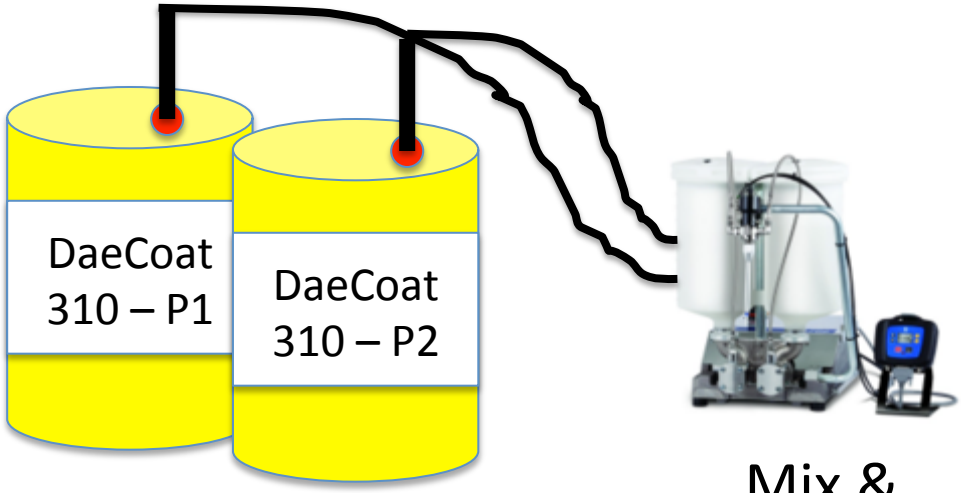
Thickness: ~20microns



Adhesive Force of DaeCoat™ 310 With Daetec's PI: DaeCoat™ 210

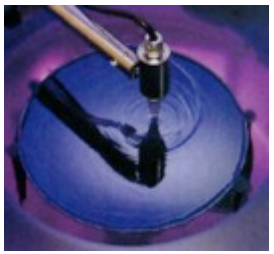


High Volume Manufacturing



drum = 200L

Mix &
Dispense
Tooling

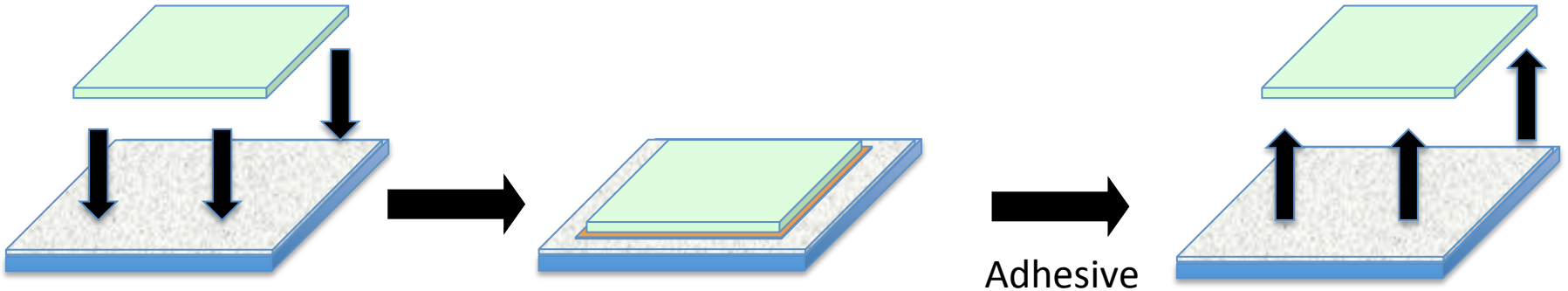


Spin Coating

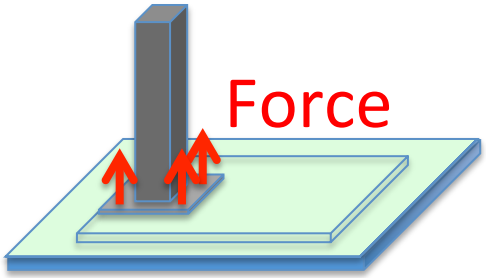
DaeCoat™ 310 components are stable for long shelf-life prior to mixing.

Glass on Glass Bonding

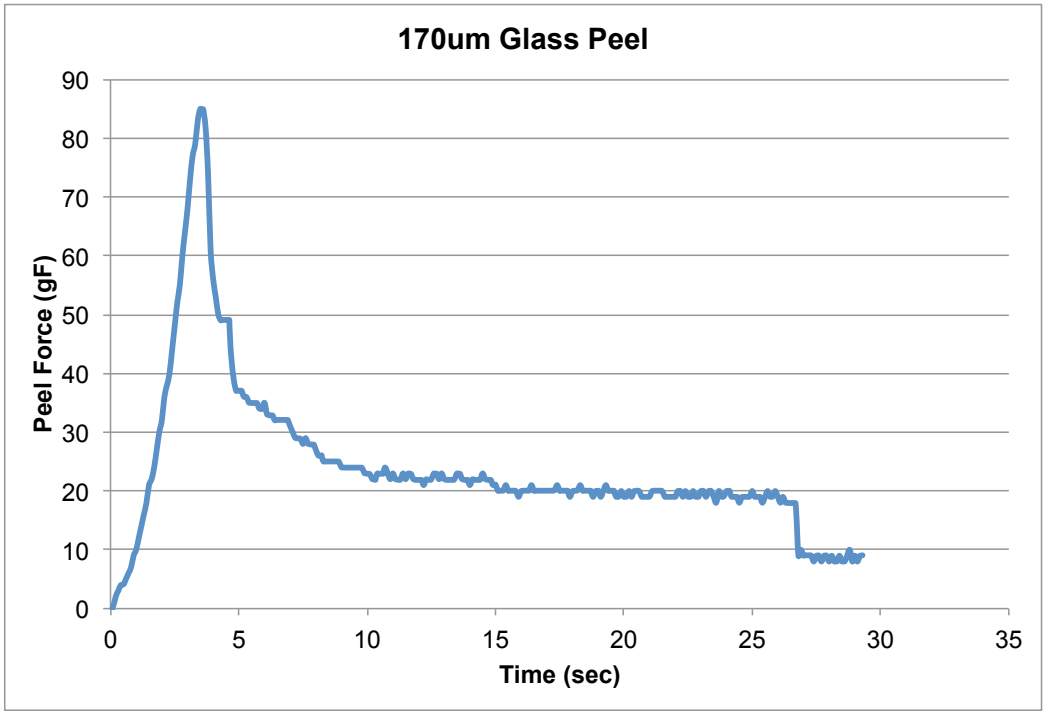
- To prevent fusion, carrier is treated
- Allows glass substrate to debond after high temp processing



Controlled Adhesion: Edge Pull



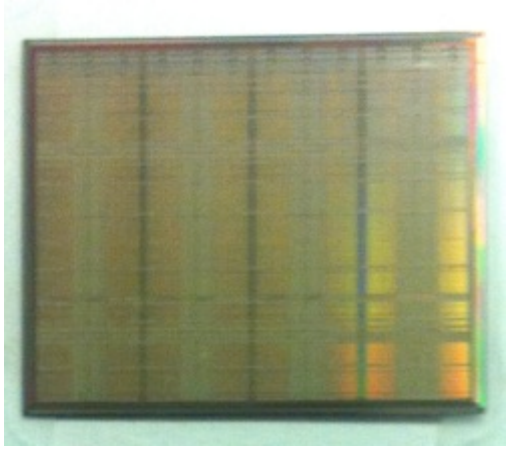
Low Bond Force Weaker Adhesive



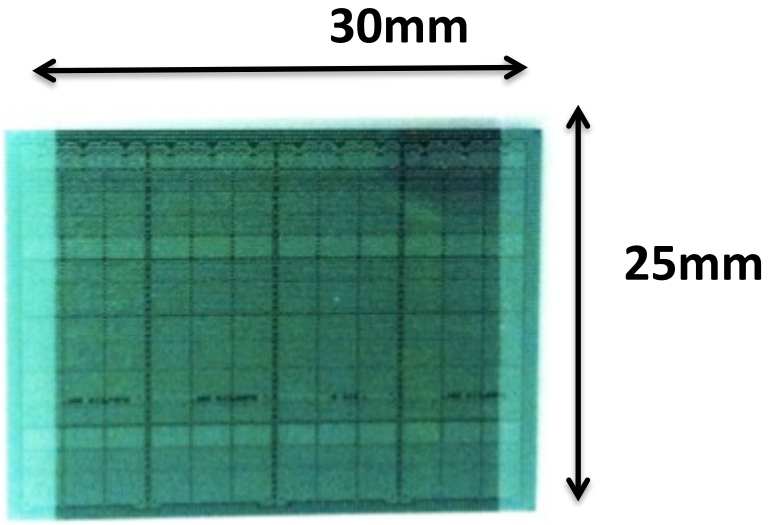
4. Devices

Thin Silicon Interposers (TSIs)

- Substrate ~100um thickness
- Underlying bumps ~100um height

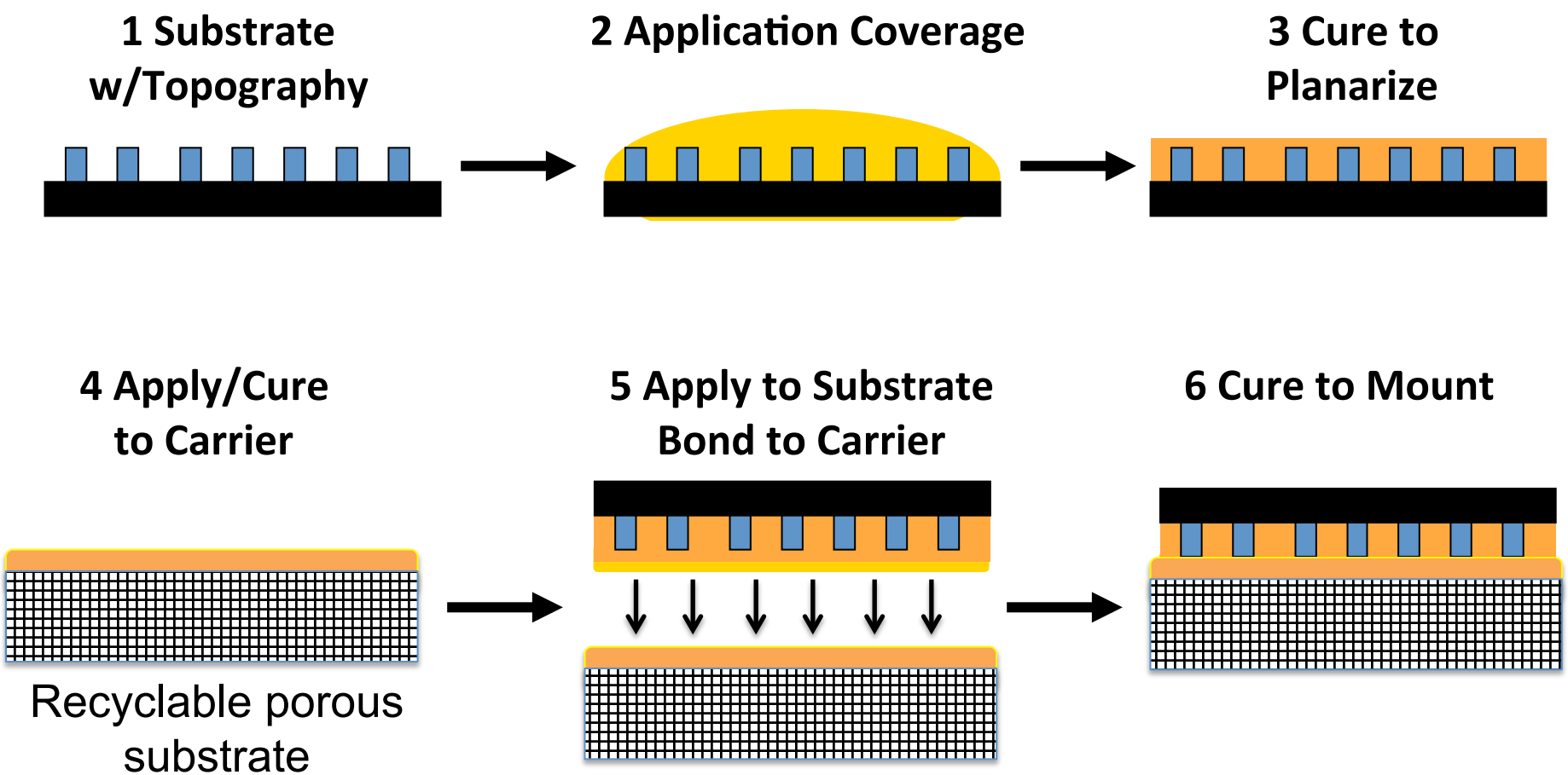


Top side



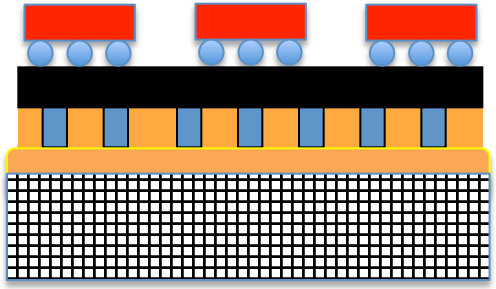
Bottom side
(contains solder bumps)

Application



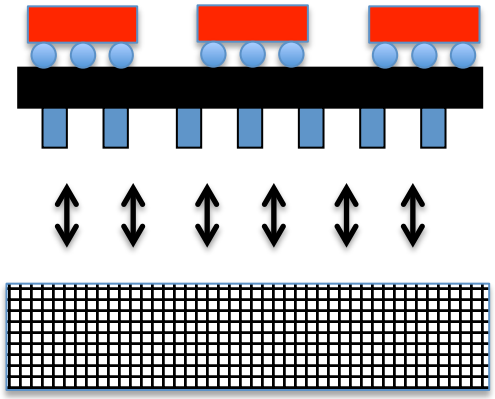
Post-Bonding Process

7 Customer Process



Bonded interposer attach chips to interposer Reflow 250-300C

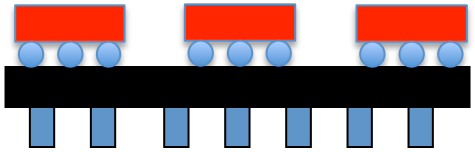
8 Debond & Cleans



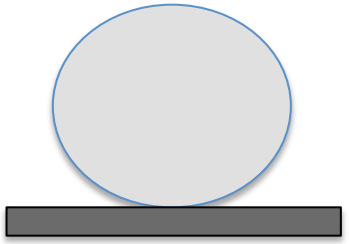
Debond and Cleans rinse, dry

Recycle carrier

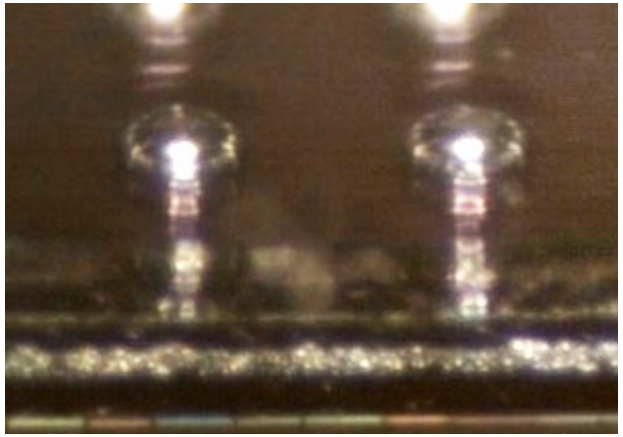
9 Acquire Final Product

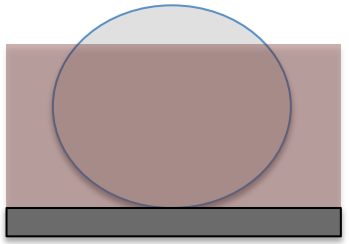


Adhesive Planarization



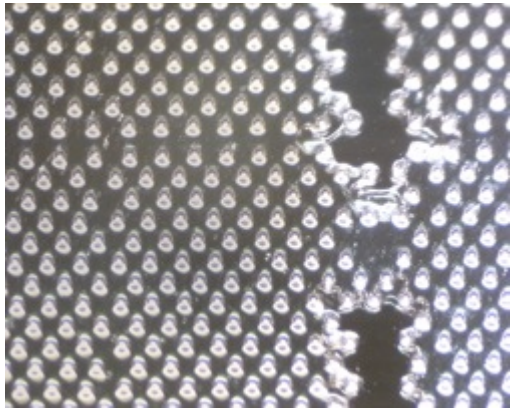
No adhesive



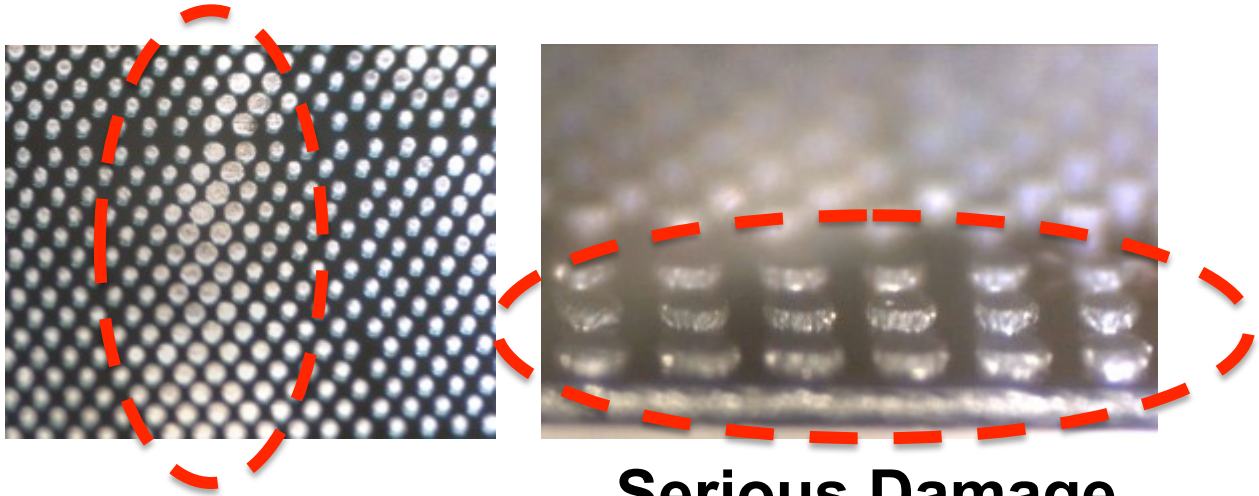


Adhesive

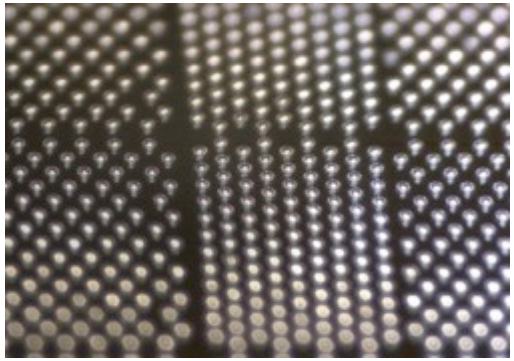
Planarization and Thermal



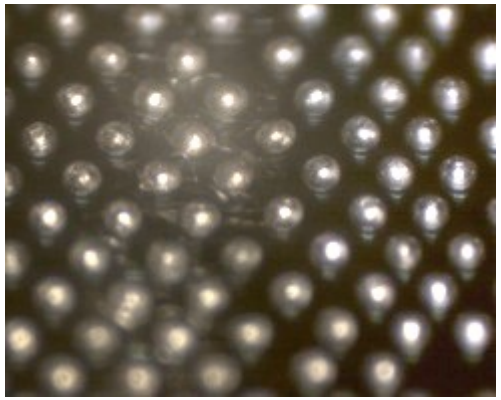
- Voids -



Serious Damage



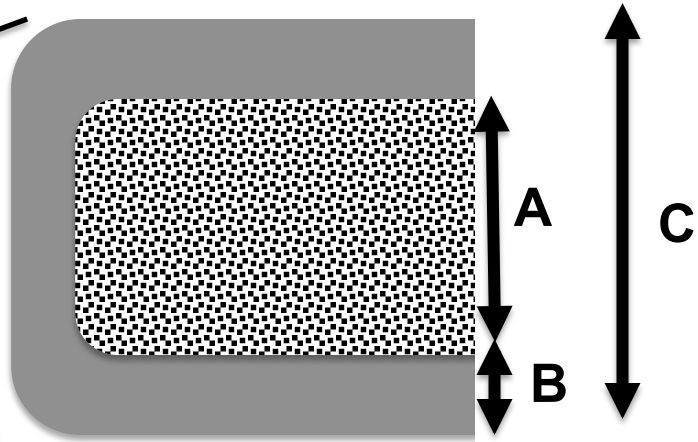
No Voids

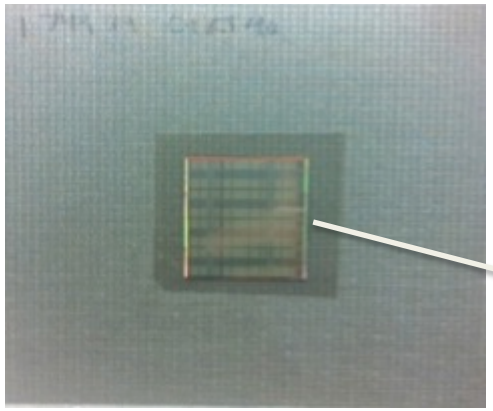


No Damage

Porous Carrier

Porosity higher for inside material (A). Outer coating (B) is lower porosity



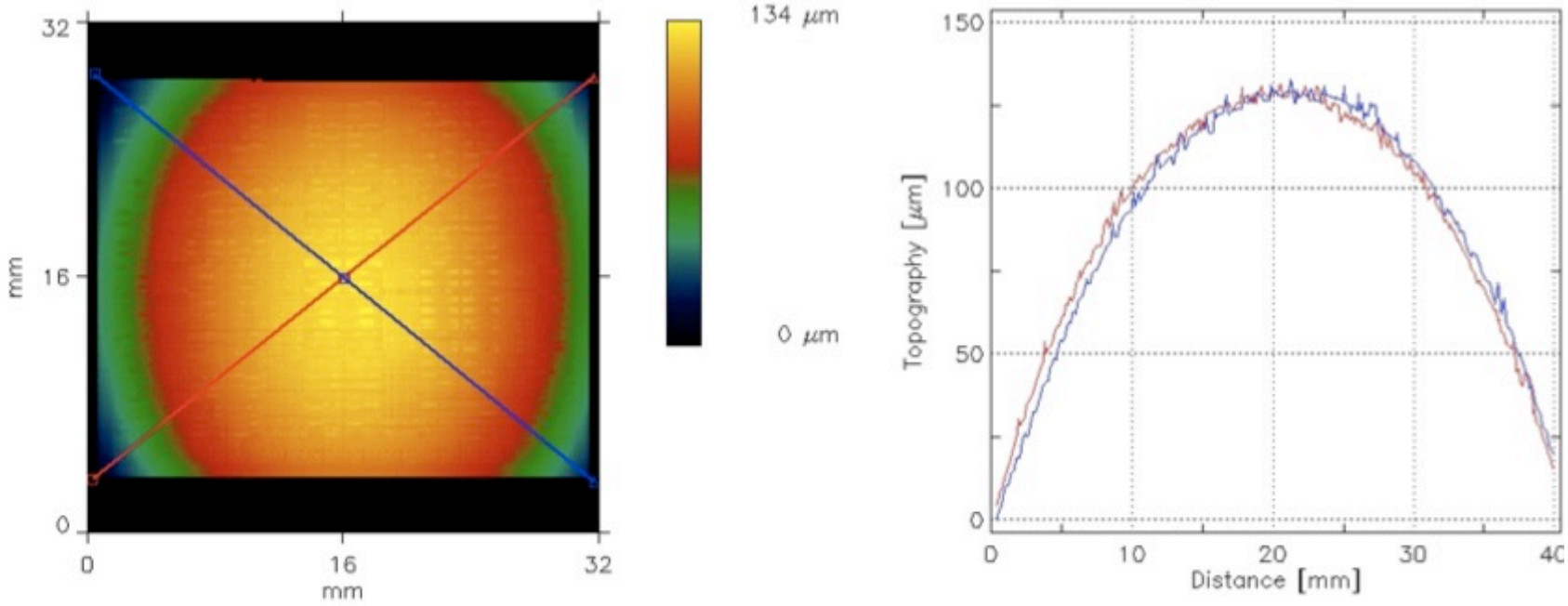


Porous Carrier

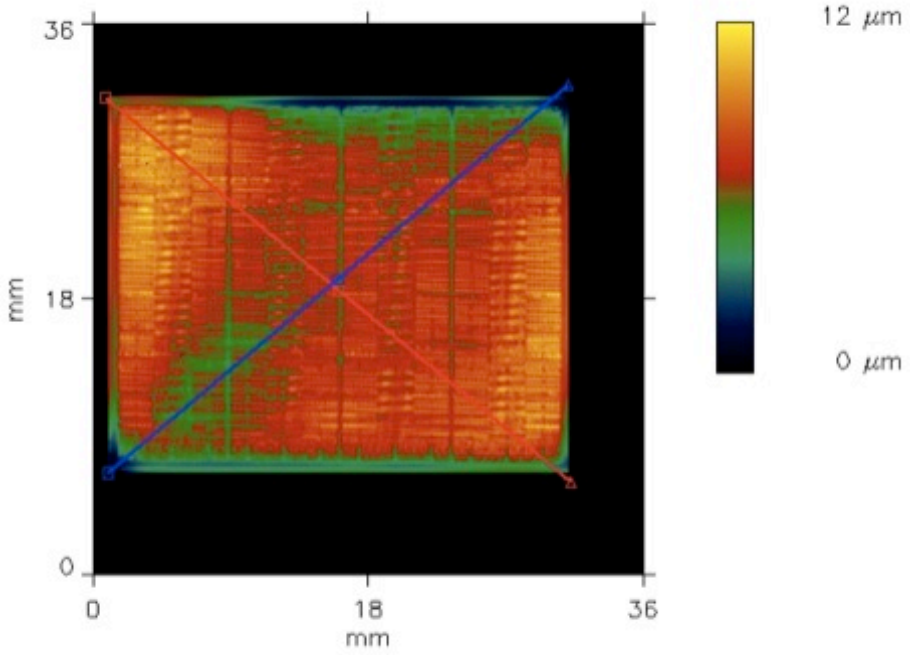
TSI on adhesive

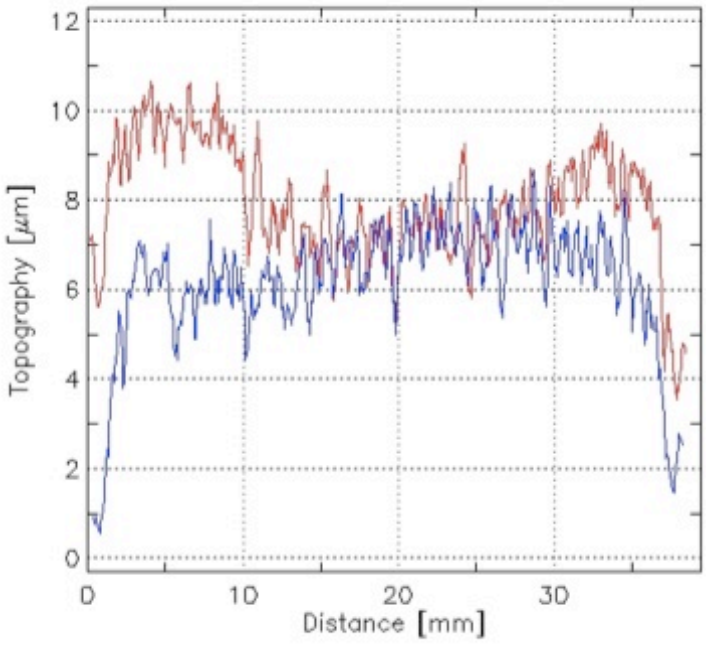
A = 0.5 – 0.8mm
B = 0.1 - 0.25mm
C = 0.5 – 1mm

Results – baseline TSI

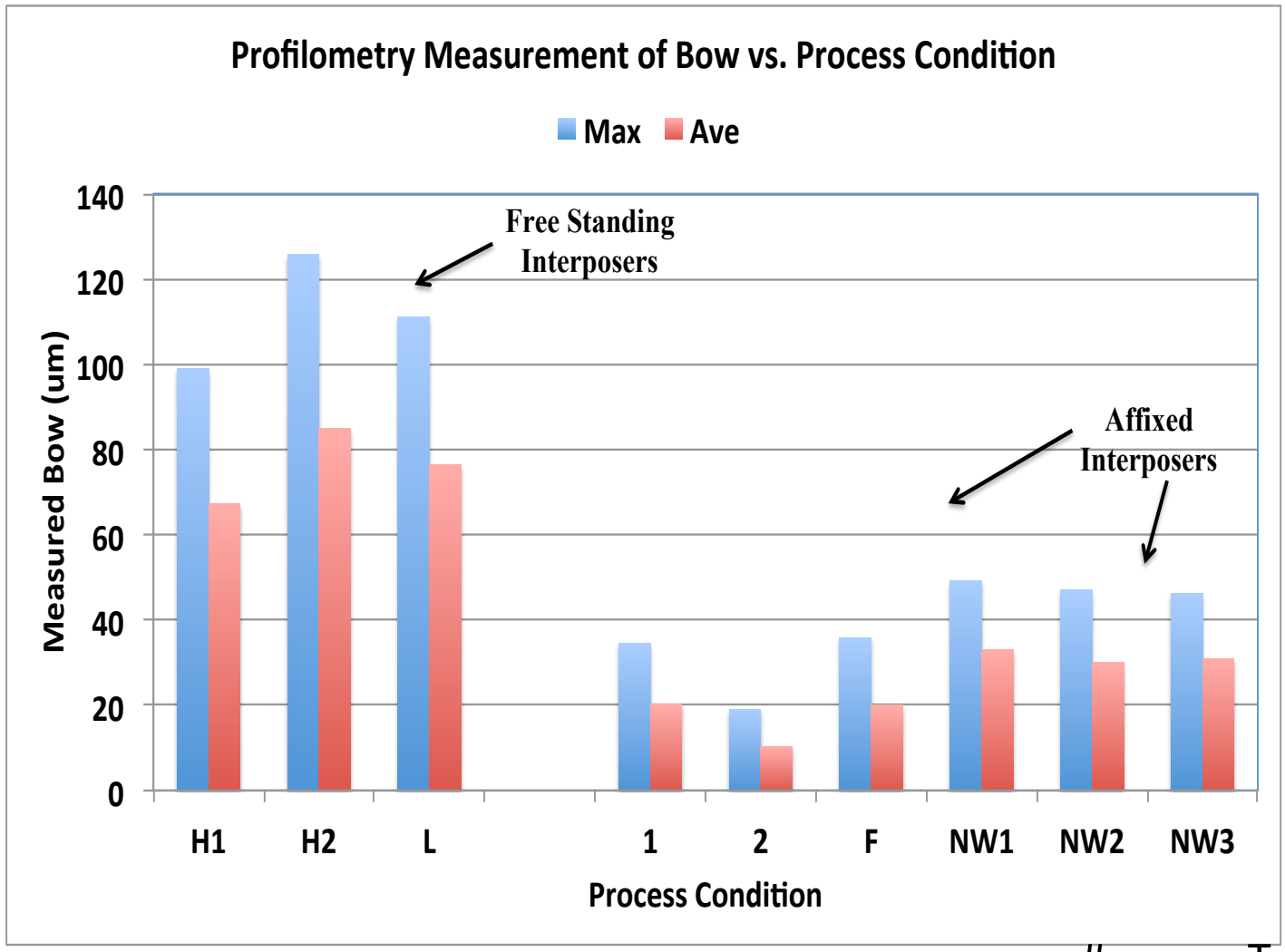


Results – Bonded TSI

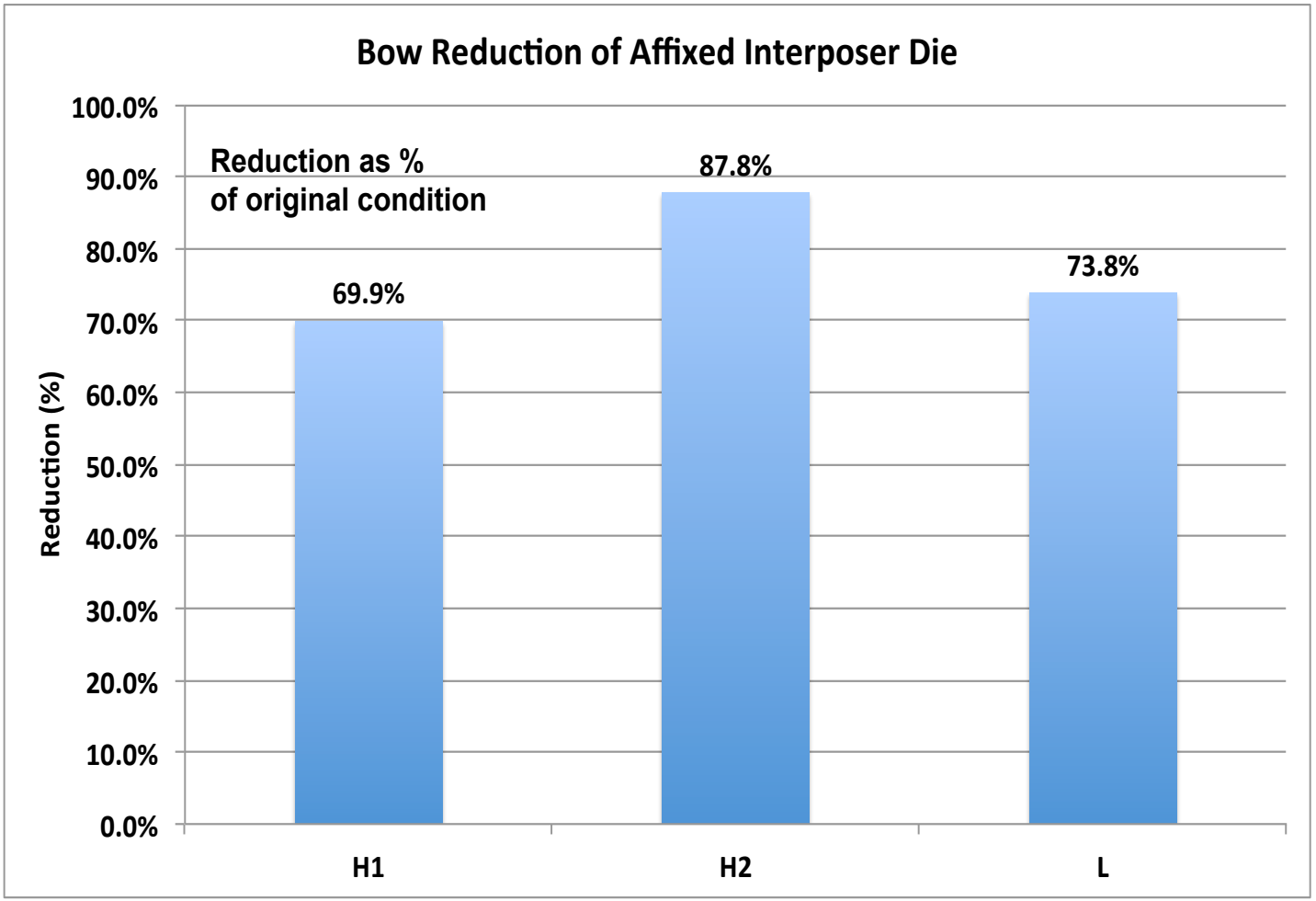




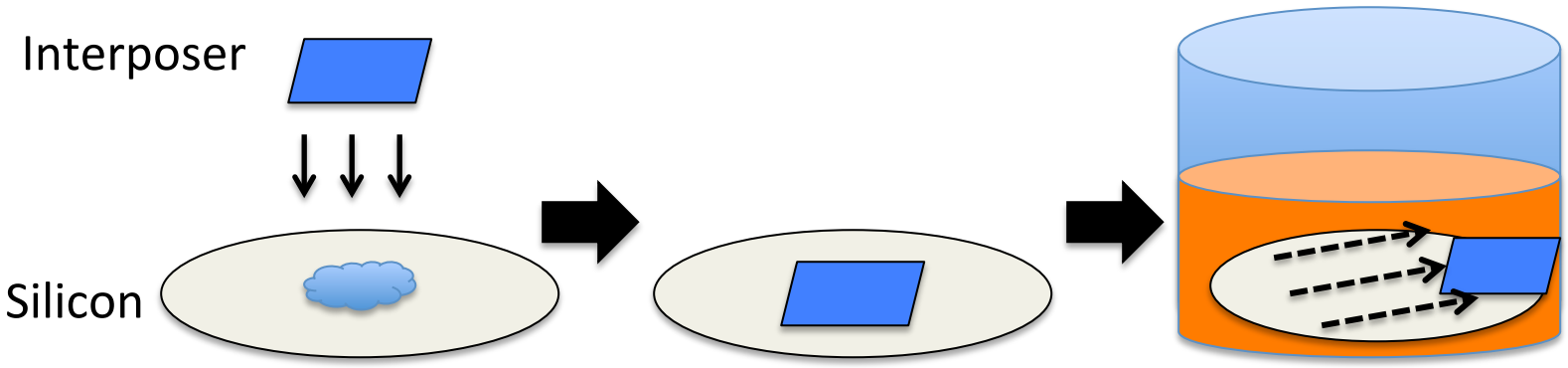
Variation <12um



#	Type
1, 2, F	Peripheral
NW	Porous Subst


Bow Reduction of Affixed Interposer Die
Reduction as %
of original condition
Reduction (%)
100.0%
90.0%
80.0%
70.0%
60.0%
50.0%
40.0%
30.0%
20.0%
10.0%
0.0%
69.9%
87.8%
73.8%
H1
H2
L

Results – DeBonding

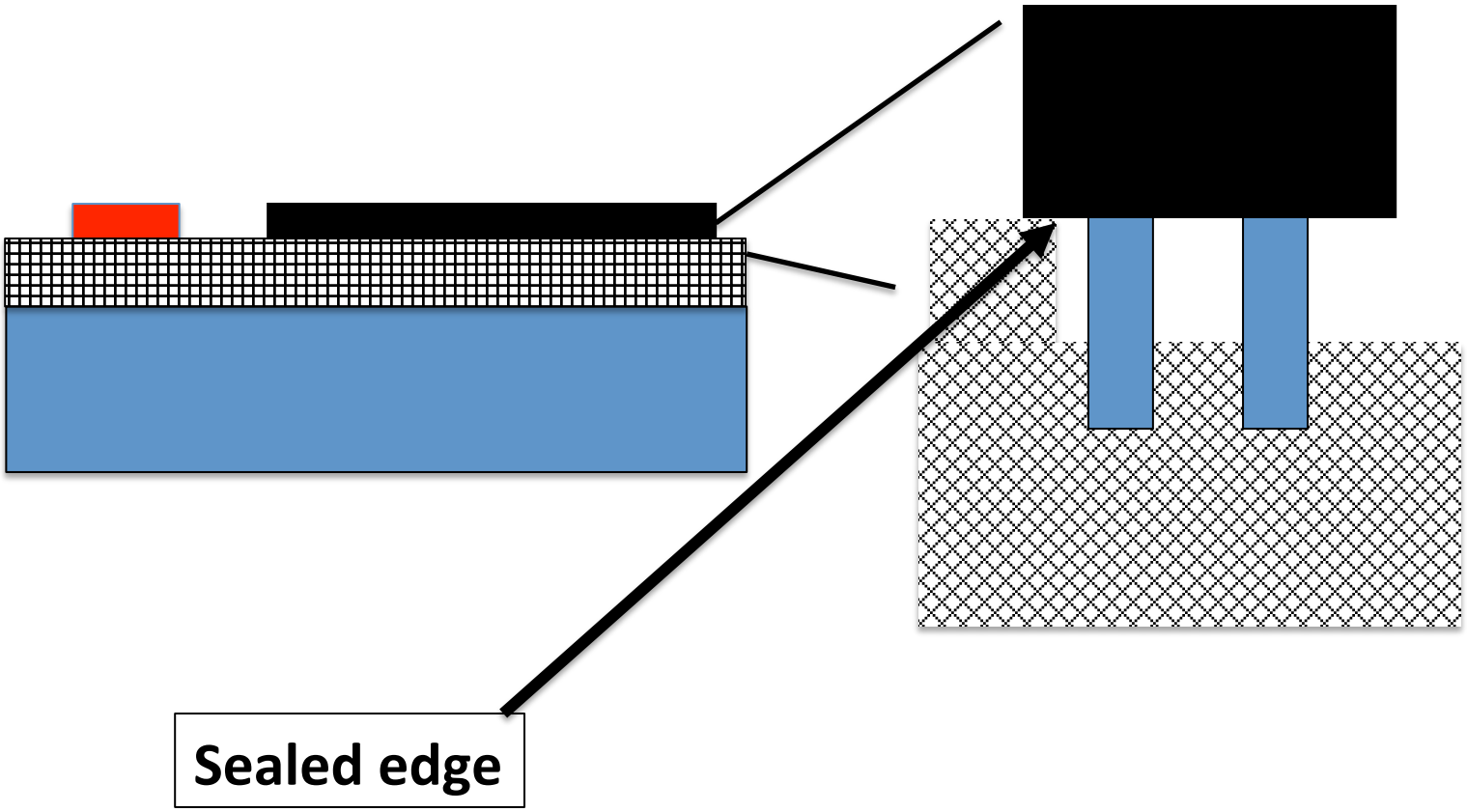


1	2	3
Prior activity involved applying adhesive to interposer & silicon wafer, holding interposer in place	Bond interposer to silicon wafer, observe flatness and other process details	Debond from silicon in Daetec digesting fluid, observe time

Devices (cont.)

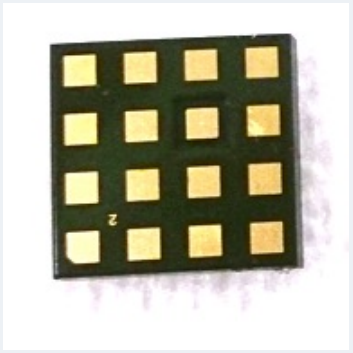
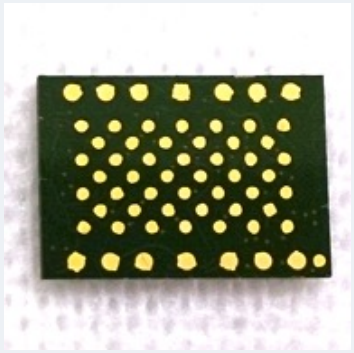
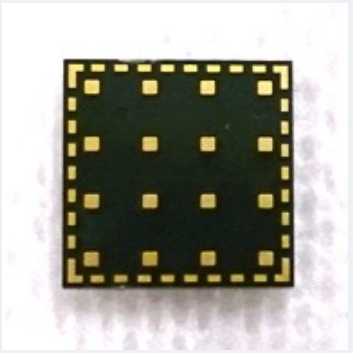
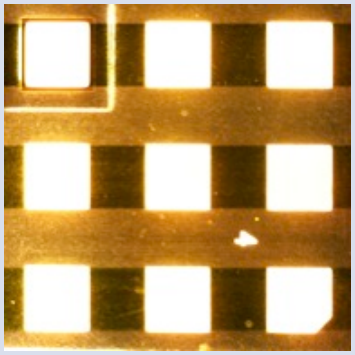
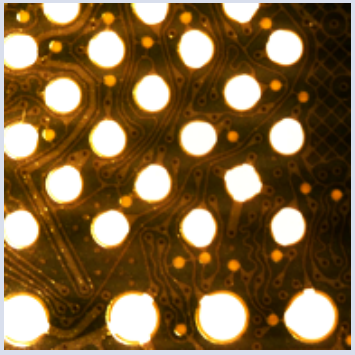
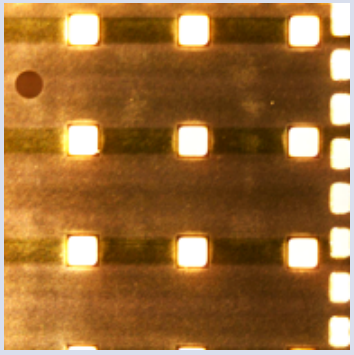
- Desire to attach device, process, remove with no residue. Adhesive is thermal & chemical resistant, conforms to device substrate
- Various adhesives are available
- Device substrates can be irregular
- Bond/edge seal (A) desired, best w/thickness
- Adhesive may be applied by several methods
- Carrier recycle with cleaning
- Total cost must be considered

Component Bonding

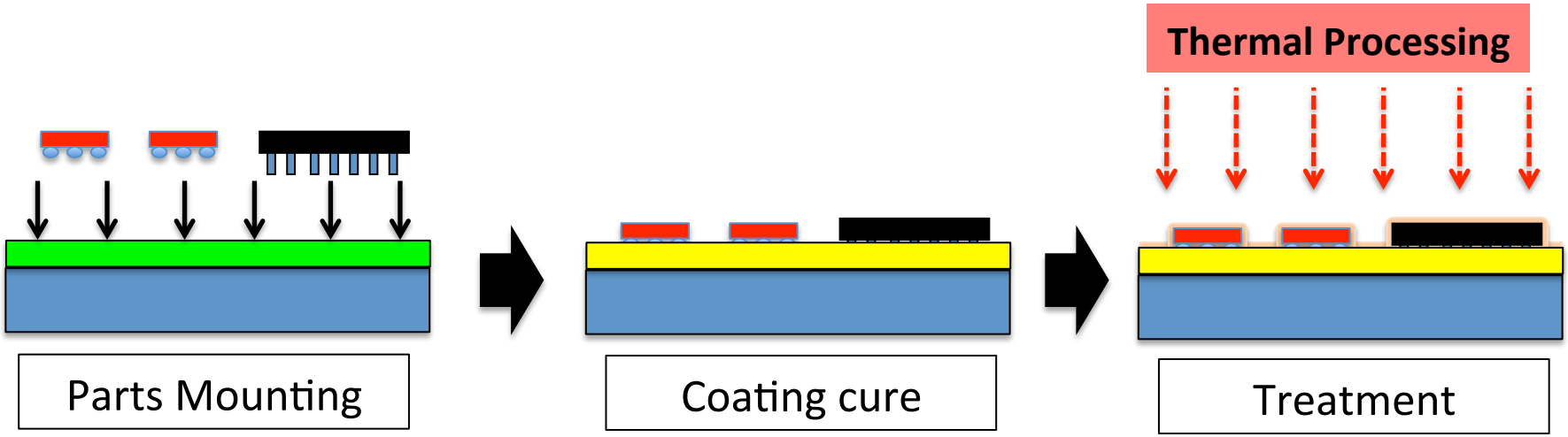


Small Devices for Thermal Processing

Appearance of Bottom

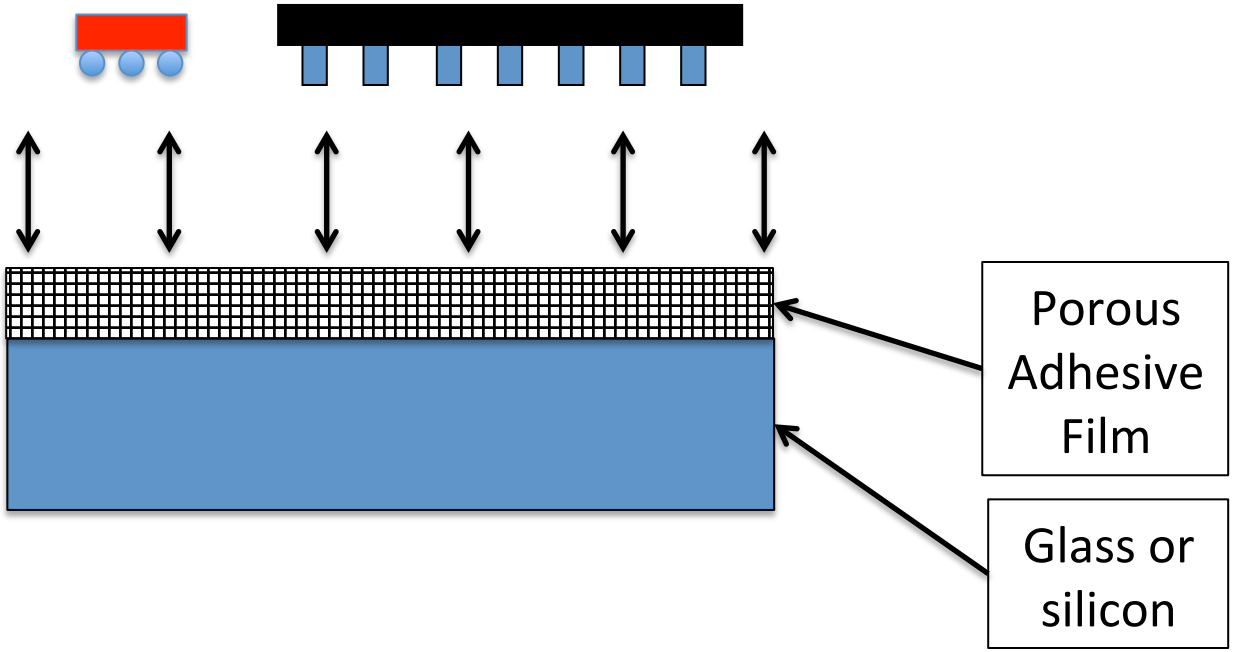
Name	#1	#2	#3
Dimension	0.95cm x 0.95cm	1.65cm x 1.15cm	0.95cm x 0.95cm
Overview			
Microscopic Picture			

Process Description

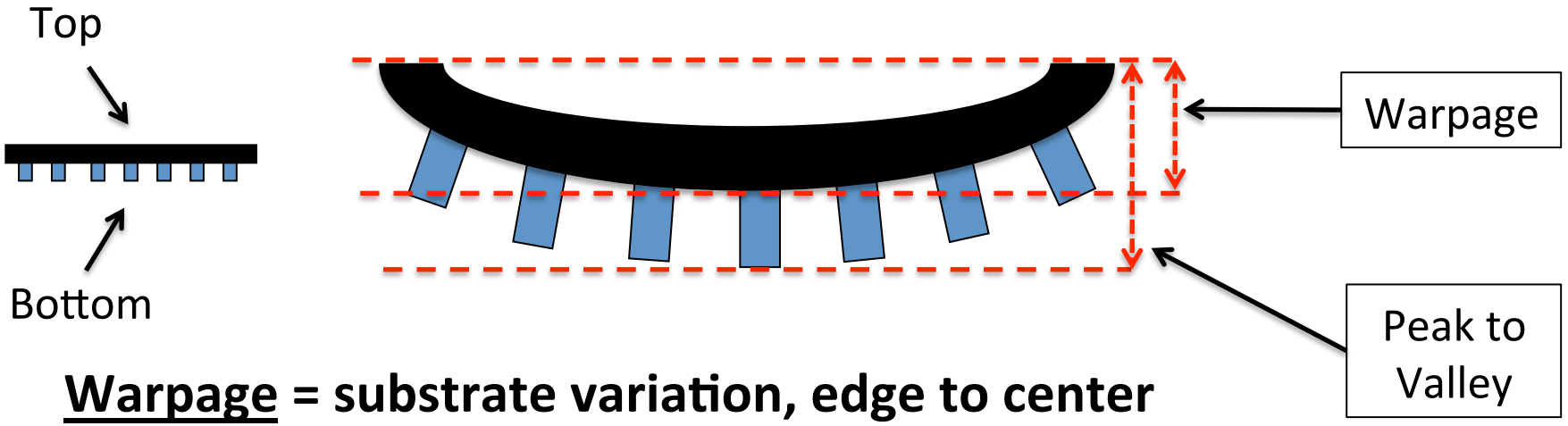


Process Description

Adhesive is applied as a film to carrier on Thick Glass, Open-Faced



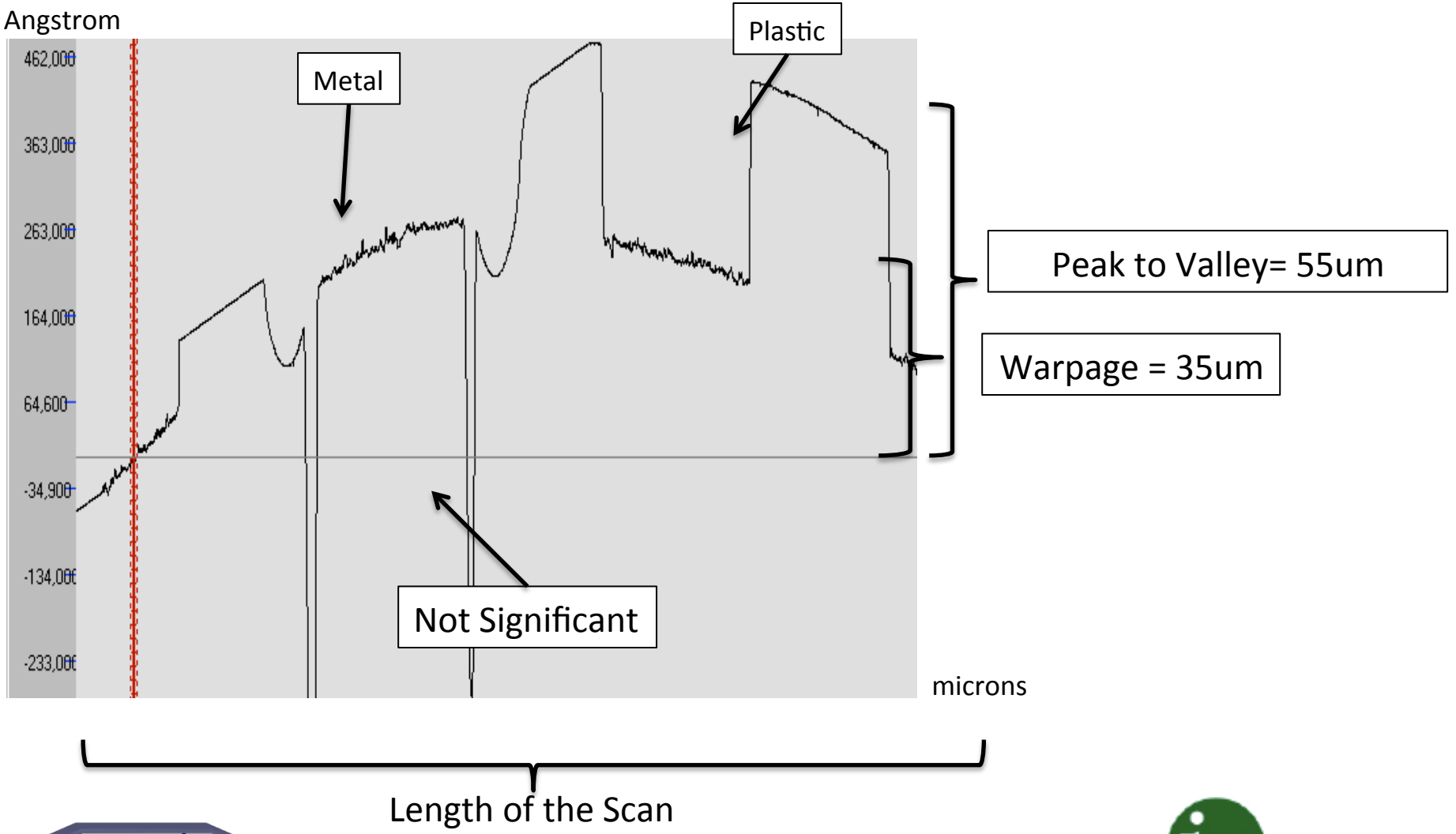
Substrate Description



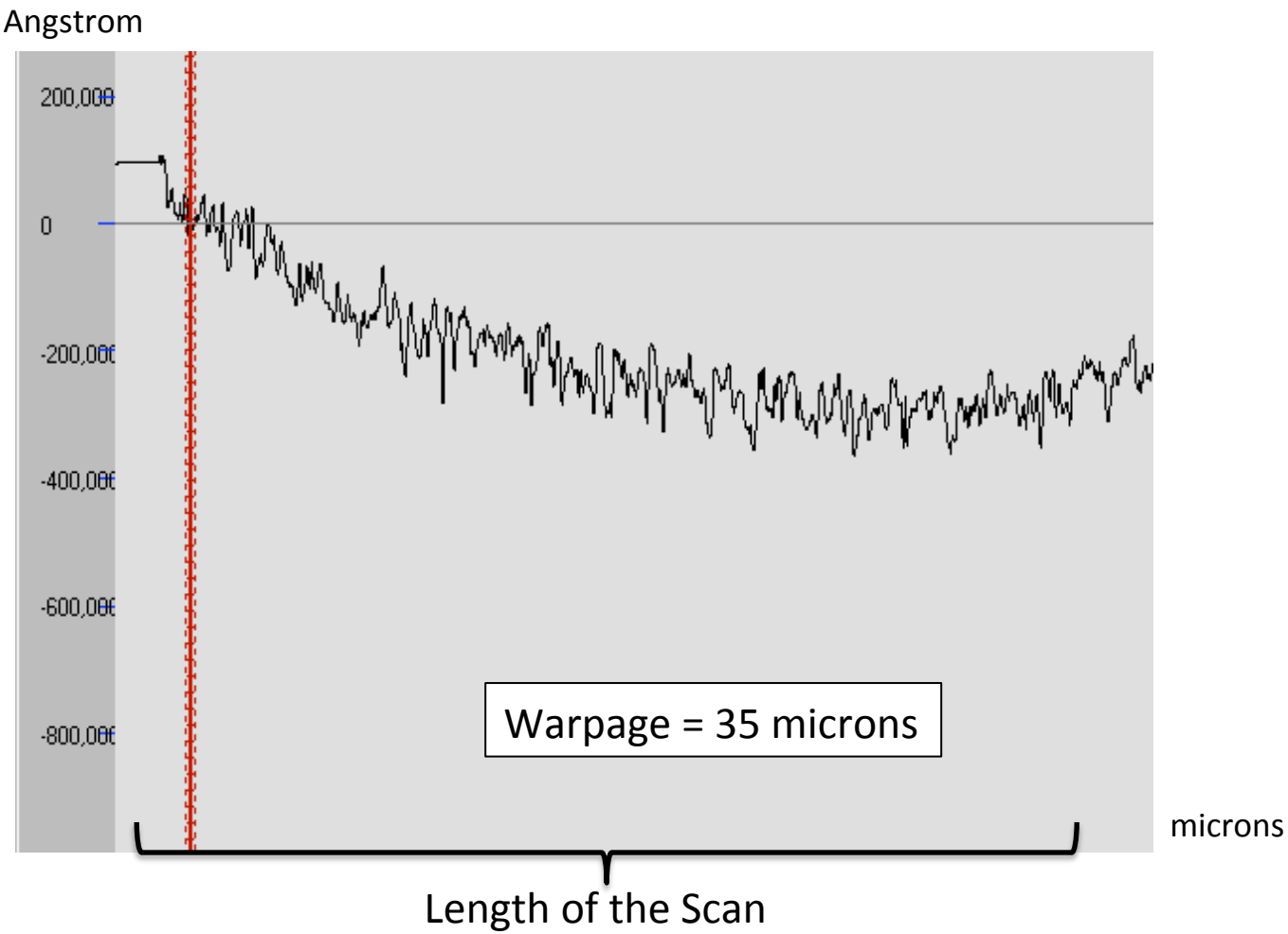
<u>Warpage</u> = substrate variation, edge to center (no topography)

<u>Peak to valley</u> = min to max (with topography)

Surface Scan (Bottom of Substrate #1)



Surface Scan (Top of Substrate #1)



Ability to Bond & Seal w/Topography

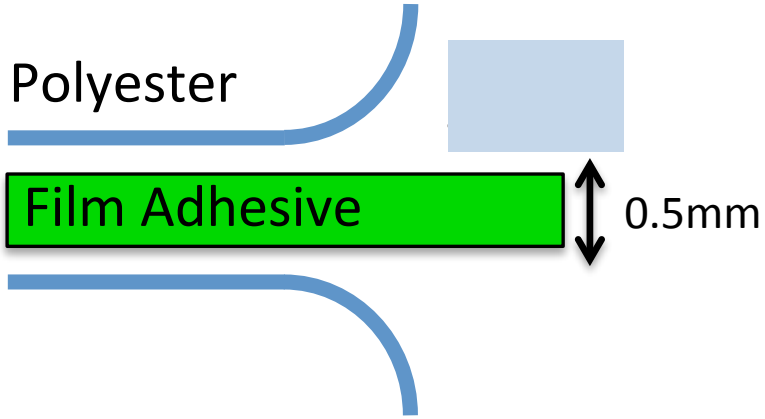
Use of various DaeCoat products

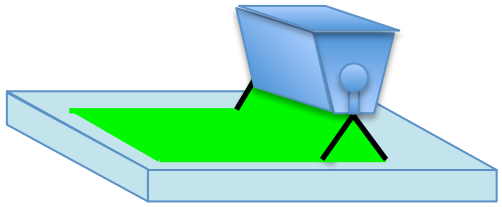
Substrate	Peak to Valley (µm)	Warpage (µm)	Adhesive thickness <60µm	Adhesive thickness >60µm
#1	55	35	B	B
#2	14	<5	A	A
#3	26	23	B	B

A= Bond + Edge Seal (Ideal Process)

B= Bond

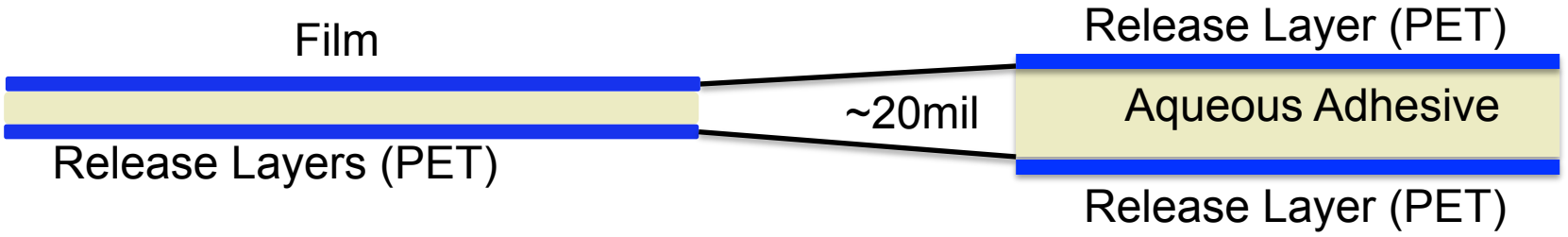
Adhesive Film - Options





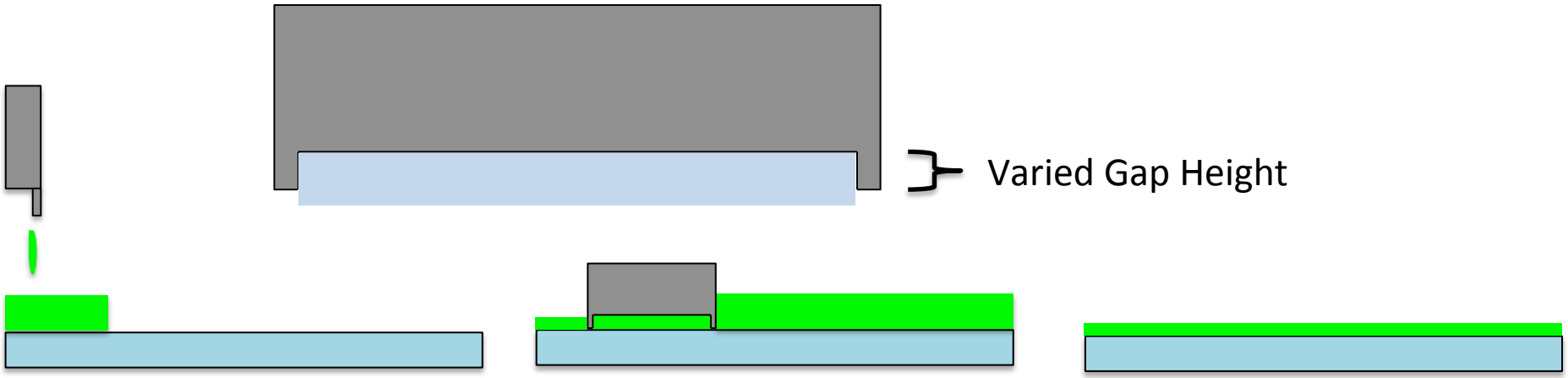
1	2
Use as B-stage film, thickness can vary	Slit-coating to substrates, SB cure, process as desired

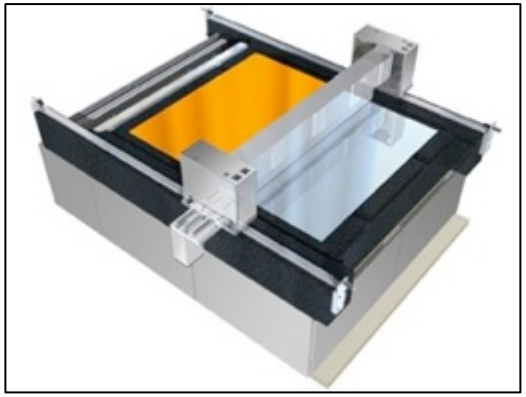
Film w/Release Layers

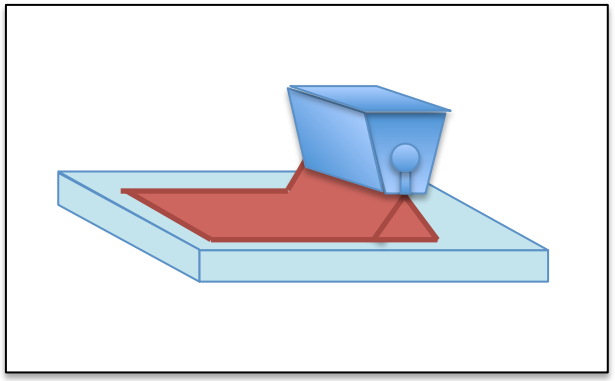


- Aqueous-based adhesive
- Thickness = 20mil ~500um ~0.5mm
- No backing
- Sandwiched between PET release layers
- Remove 1st PET liner, apply to substrate
- Use a rubber roller, apply exposed adhesive to substrate, increase pressure onto PET facing up, remove 2nd PET liner, proceed with bonding

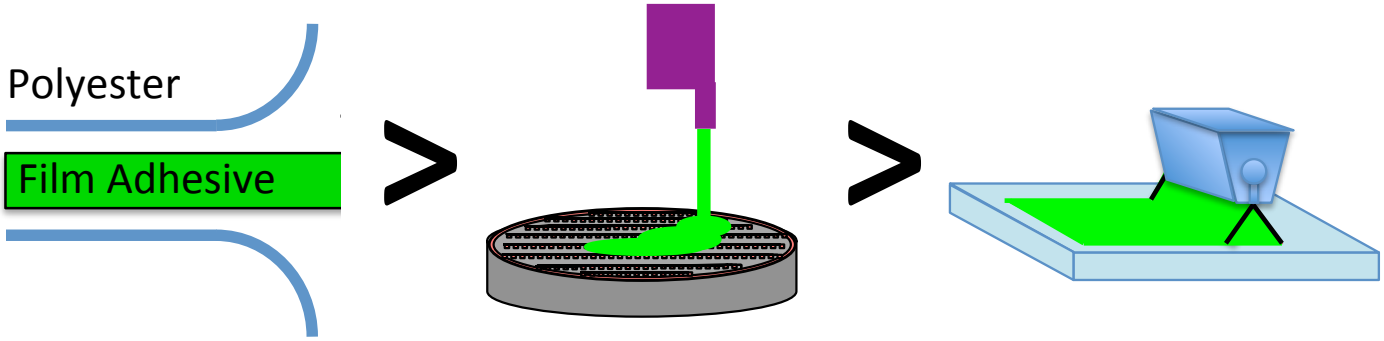
Slit Coating







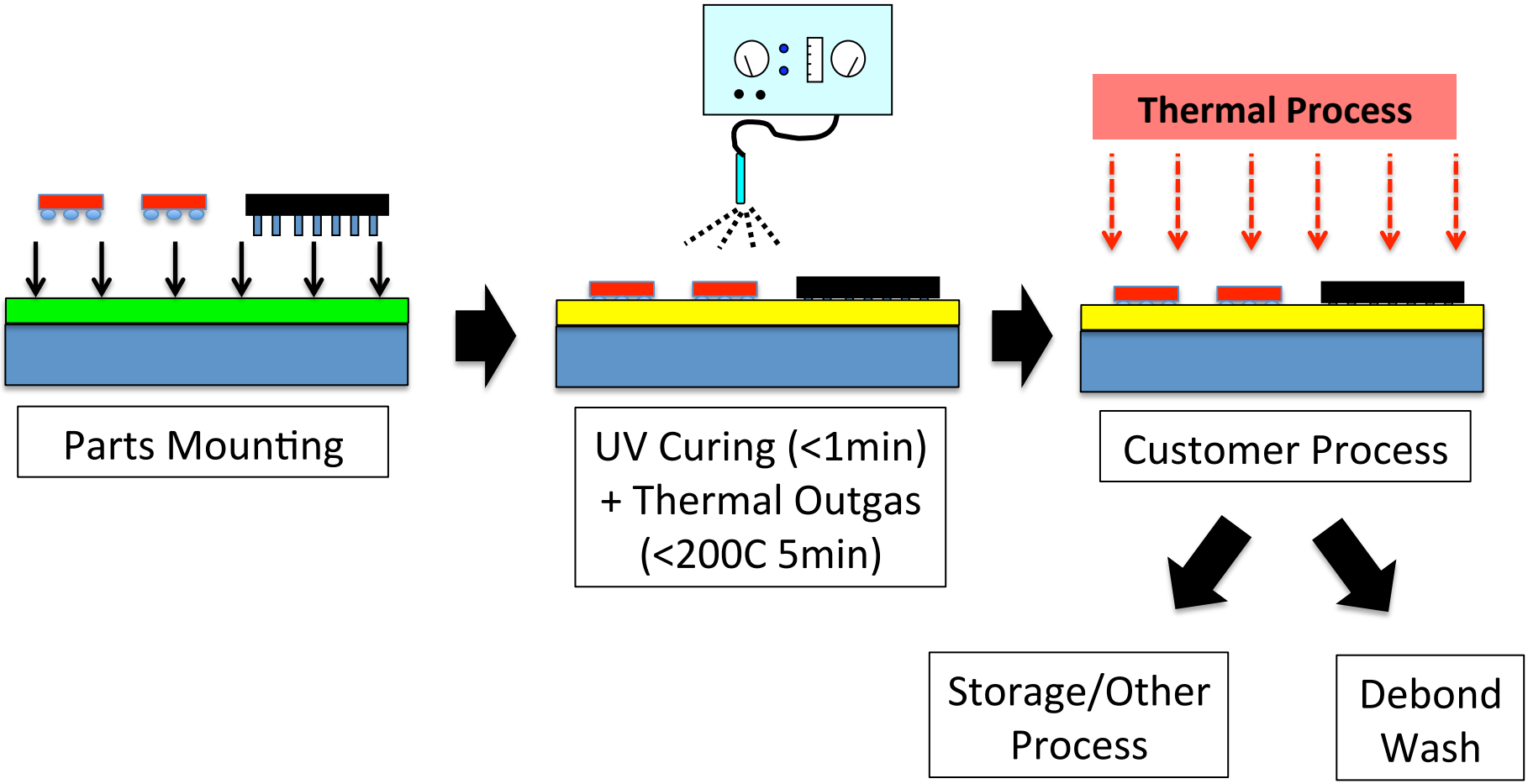
Cost Considerations



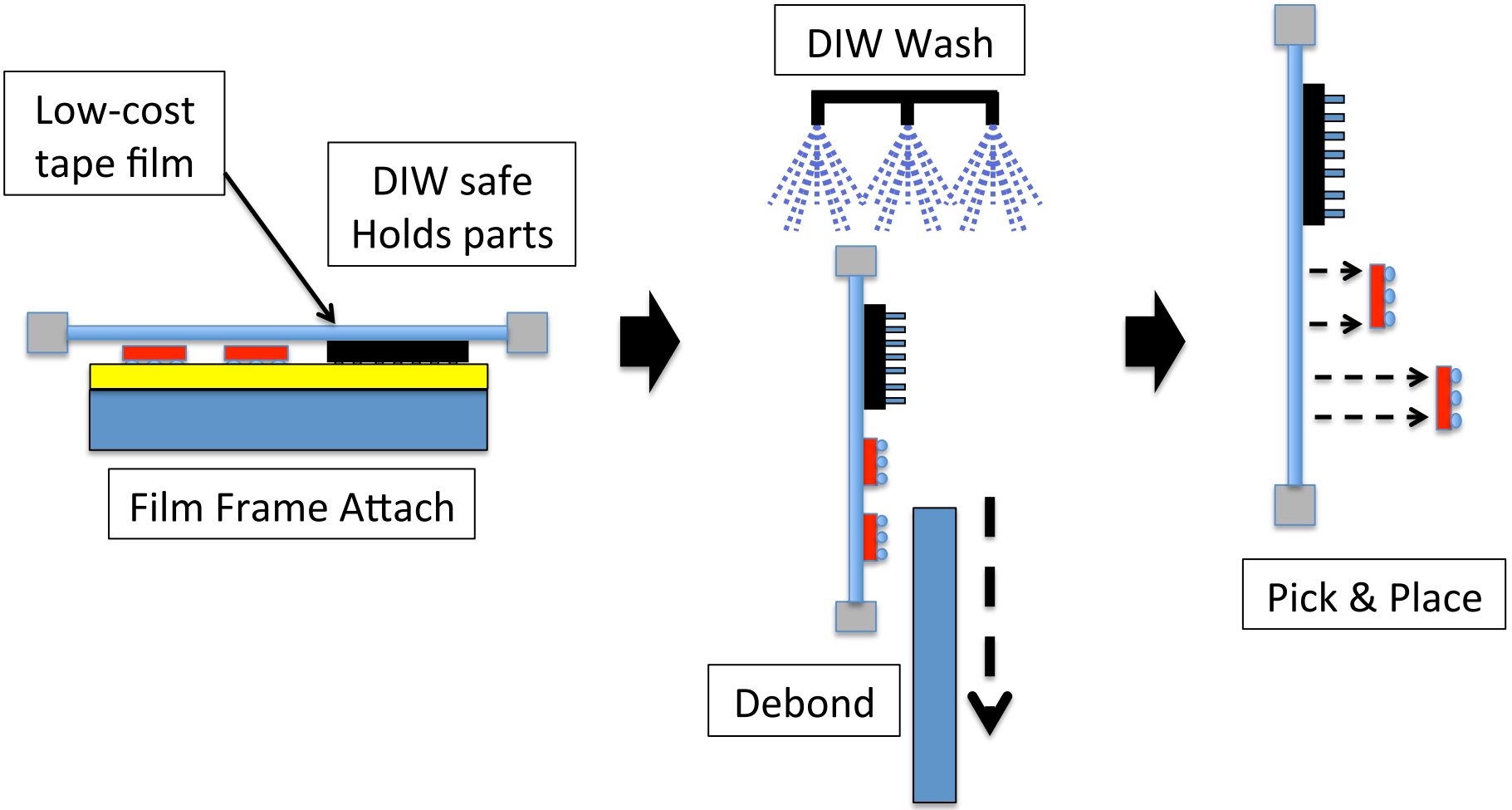
Parameter	Film w/release liners	Spin Coating	Slit Coating
Coating solids (%)	80-100	<100	100
Cost ($/cm2)*	<0.05	<0.05	<0.02
Convenience	High	Med	Med
Tool Required	-none-	coater	coater

*assume best case conditions with max solids for coating capability

UV Cure Film/Coating



Debond/Rinsing



Summary

- Temporary bonding technologies are being used for wafers, displays, and devices
- Key practices include variations around peel practices
- Cross-pollination continues to drive more creative development in different markets
- Improved yield, cost control, and simplicity are drivers

Contact for More Information

- DAETEC provides development, consulting, and technical training/support to solve manufacturing problems and introduce new options of doing business.
- Diversified Applications Engineering Technologies (DAETEC)

  Camarillo, CA (USA) (805) 484-5546

  jmoore@daetec.com; www.DAETEC.com