

High Value Thin Wafer Support Technology for 3DIC

Jared Pettit, Alman Law, Alex Brewer, and John Moore

Daetec, LLC

1227 Flynn Rd., Suite 310

Camarillo, CA 93012 USA

jmoore@daetec.com, www.daetec.com

Abstract

As the 3DIC market matures, more is understood about the technical and cost challenges [1]. At the 2013 Semicon-West gathering, a panel of global experts identified these technical challenges to represent some of the most significant barriers to the industry's efforts to maintain progress with Moore's Law [2]. Searching and achieving high value manufacturing of 3DIC devices requires wrestling with several technologies and processes, all which may assert a different value for the manufacturer [3]. Current technologies for thin wafer support use a wide range of adhesives applied to the device wafer, bonded to a carrier, backside processed, and de-bonded by an array of methods. Daetec has been investigating temporary bonding for nearly 15yrs, is producing a range of products for semiconductor (e.g. WaferBond™ (Brewer-Science, Inc.)) [4], and for the display market using a low-cost tunable adhesion-force material that is peeled by simple means [5]. Daetec has developed a new technology, DaeBond 3D™, allowing de-bonding to occur in a batch process while thinned wafers are affixed to film frames. This new approach provides a shift in conventional practice. Our paper presents several temporary bonding options with DaeBond 3D™ in an effort to define value-added approaches for thin wafer handling.

Key words: adhesive, temporary bonding, de-bonding, thermal resistance

I. INTRODUCTION

The combined semiconductor and display industries generate over \$600b in annual revenue. A key driver is the growth in smart phones and tablets that require higher power devices, functionality, miniaturization, and low cost. Heterogeneously stacked thin substrates are connected by through silicon vias (TSV) and solder bumps to create a three-dimensional integrated circuit (3DIC). Demand for these devices is growing at 2X the rate for conventional silicon (Fig. 1).

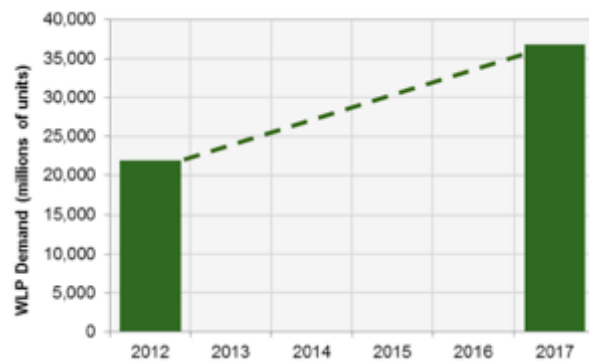
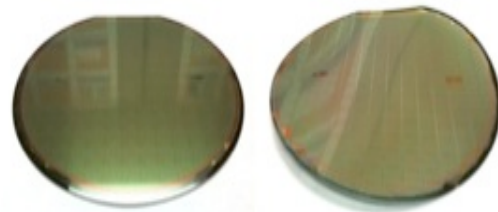


Fig. 1. Demand for WLP units >20% CAGR.

Making 3DIC devices requires multiple processes to prepare wafer substrates such that thin die can be stacked and connected. Some processes require thermal resistant polymers that must sustain temperatures exceeding 300°C for periods of several hours. All thin wafer handling processes use a rigid carrier to help prevent wafer bow and warp that is common during thinning (Fig. 2).



Before (~700um) Thinned (~100um)

Fig. 2. Effects of thinning are seen in a sapphire LED wafer at full thickness (left) and thinned (right).

Temporary adhesive is commonly applied to the device wafer, whereby it is then bonded to a carrier, processed, and then de-bonded and cleaned (Fig. 3). A range of polymers have been reported for thin wafer handling, including rosin-urethane [6], silicone [7], rubber [8], and acrylic [9].

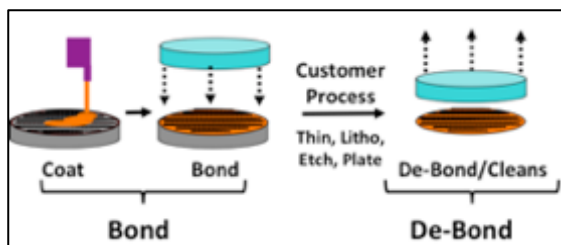


Fig. 3. Bonding and de-bonding (includes cleans).

Several adhesives are marketed for 3DIC, all involve the same application and bonding, however, their main variance is in de-bonding (Fig. 4).

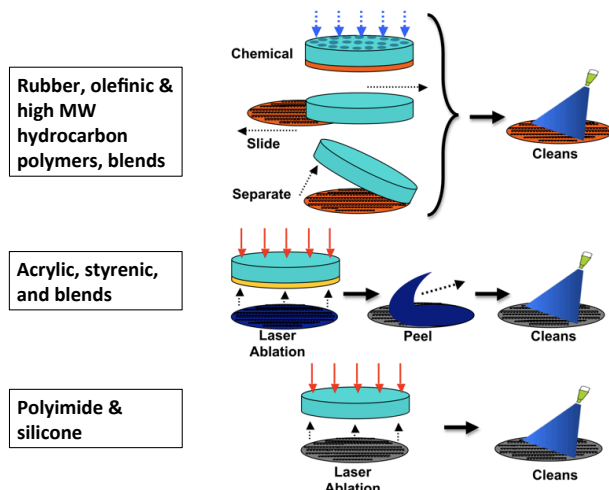


Fig. 4. Leading adhesives for 3DIC with varying complexities in de-bond performance.

Customers faced with the challenge of harnessing 3DIC's benefits must decide which thin wafer handling technology enables the manufacturing of their product. No technology currently exists that fits all applications. Defining what is high value is dependent upon factors germane to the customer and their product.

A. High Value Thin Wafer Support

Many properties exist to measure value in adhesive technologies. Choosing an adhesive will likely also include a knee-jerk de-bond method. For example, a low temperature thermoplastic adhesive may simply be de-bonded by thermal sliding or chemical dissolution, whereas a thermoset likely requires laser ablation (Fig. 4). Such properties include thermal resistance, thickness, cleaning ability, de-bonding practice, tool requirement, and cost. Additional criteria may include the "green" nature of the process and strategy associated with single-wafer or batch processing. A few properties are discussed here, representing key interests in the marketplace and attempts to achieve a simple and robust practice.

B. Thermal Resistance

One of the highest thermal resistant polymers available in commerce, polybenzimidazole (PBI), has

been formulated into several coatings and adhesives [10]-[12]. Such materials are chosen to support simultaneous high vacuum with thermal conditions. High glass transition (T_g) materials (crystalline) outgas lower when the thermal condition is below their T_g , and if amorphous, below their softening point (SP), as described below for a CVD (Fig. 5).

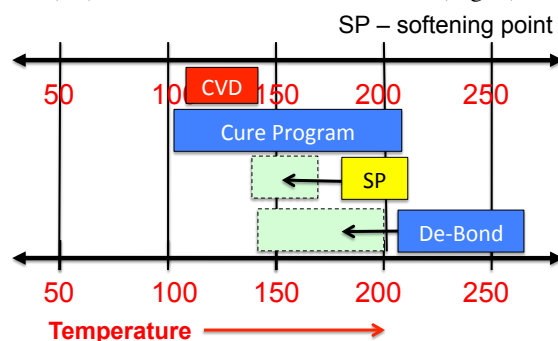


Fig. 5. Material selection using SP > process (CVD).

Alternatively, barrier materials may be added to suppress the migration of gaseous by-products. Barrier polymers are macromolecules, restricting the passage of gases, vapors, and liquids [13]. These substances exhibit low permeability as expressed as the measured gas passing through a specific polymer film of given thickness per day at 1 atm pressure (cm³-ml/day-atm). Experiments indicate barrier values of 10% offer a measured benefit in support of CVD processes (Fig. 6)

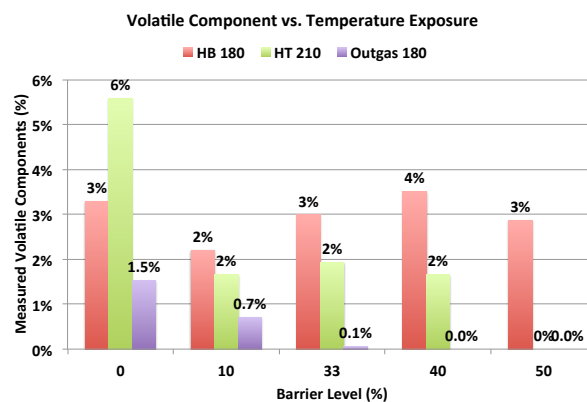


Figure 6. Outgas vs. barrier % in a CVD operation.

C. Batch Debonding

As a departure from the complexities and cost of single-wafer tools, bonded wafer stacks that are adhered onto taped film frames (carrier side out) are assembled in a cassette and then immersed into a cleaning solution. Penetration occurs through a variety of means to cause compromise to the adhesive and subsequent carrier removal. Cleaning occurs simultaneously in the same bath. Batch processing and cleaning of the entire cassette occurs typically within 15min.

C. Green Products

As the electronics market explores ways to reduce the use of chemicals that increase risk from exposure to personnel or the environment, more products are entering the supply chain to meet this need. Many of Daetec's products are 100% solids (solvent free), use water to apply or process, and reduce environmental risk. Some examples include washable coatings that planarize a wafer surface (DaeCoat™ 515), protecting its features including bumps over 100um, and will rinse away after a process (Fig. 7).

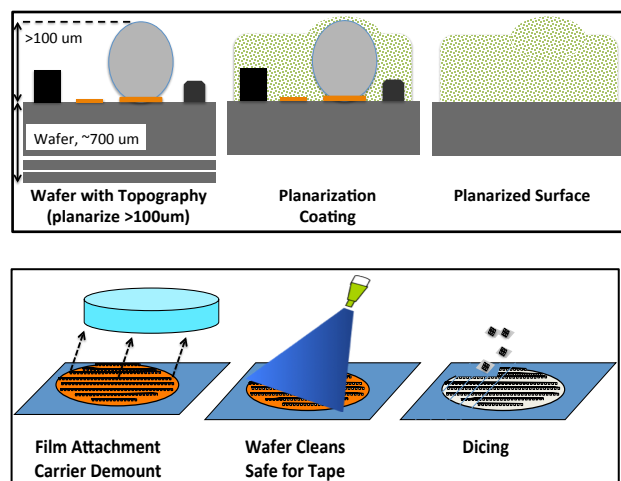


Fig. 7. DaeCoat™ 515 washable planarizing coating.

A variation of the planarizing coating is DaeCoat™ 550 UV-cured water rinsed coating to remove debris from the laser induced heat activation zone [14]. The product is simply applied to the surface and washed after the laser process is completed (Fig. 8).

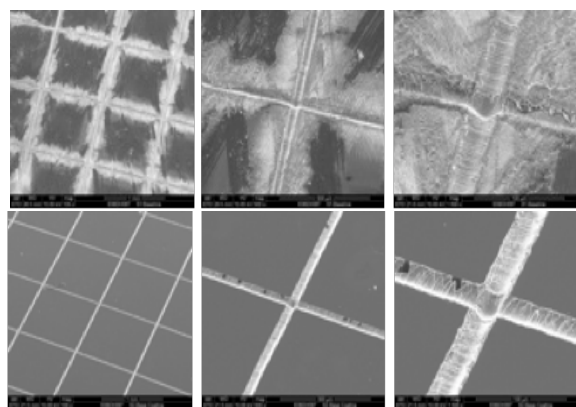


Fig. 8. SEM photos of laser processing without DaeCoat™ 515 (top) and with coating (bottom).

D. DaeCoat™ Temporary Bonding Products

To assist with the determination of high value properties for a specific temporary bonding process, a list of products is given in Table 1.

Table 1. List of temporary bonding products, stable to >350°C, unless indicated otherwise.

DaeCoat™	Description
200	Transparent film; peel de-bond
210	Polyimide film; peel de-bond
310	Tunable adhesive for polyimide; peel de-bond
350	Coating w/tunable adhesion
515	Water washable
550	UV cured, water washable
615	Thermoplastic, stable to 200°C, detergent washable (DaeClean™ 150)
620	Thermoplastic, stable to 250°C, detergent washable (DaeClean™ 150)

These products enable multiple approaches to temporary bonding thin and fragile substrates. Temporary bonding products are used for flexible organic light emitting diode (OLED), thin glass, foils, wafers, and components (die). Table 2 describes the work unit types, application, DaeCoat™ products, and the suggested configuration to be used.

Table 2. Applications of DaeCoat™ products.

Work Unit	Market	DaeCoat™	Method
Organic Film	OLED, flexible displays	350	Cure on carrier, bond w/pressure
Organic Film (cast)		310	Cure on carrier, cast & cure liquid
Thin glass	TFT LCD	350	Cure on carrier, bond w/pressure
Foil	OLED, flexible displays	350	Cure on carrier, bond w/pressure
Wafer	3DIC	350, 615, 620	Planarize wafer w/550, cure on carrier, bond w/pressure
Die (chip)		350	Cure on carrier, bond w/pressure

With the possible exception of wafers, all work units mentioned in Table 2 are de-bonded by peeling practices. In most cases, DaeCoat™ 350 is used with proper adhesion adjustment to allow simple and non-damaging practices to occur. The work unit is not cleaned as the adhesive remains on the carrier allowing for possible recycling by sending the coated carrier back through the line for bonding to another work unit. An example is given of a flexible display process flow peeled from a laser trimmed glass

carrier (Fig. 9) using a roll-style tool (Fig. 10).

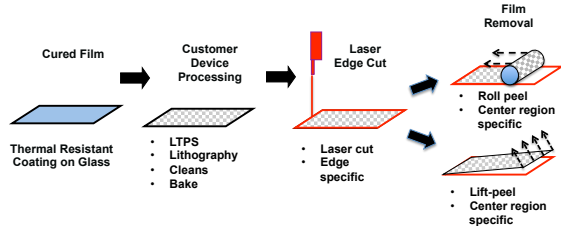


Fig. 9. Example process flow for temporary bonding of thin films in display manufacturing.

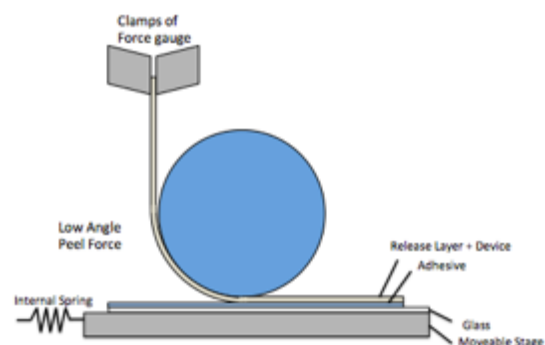


Fig. 10. Peeling model using roll-style tool.

D. DaeBond 3D™

Using similar materials as described in Tables 1&2, DaeBond 3D™ describes a novel batch-processing thin wafer handling system. Device wafers are planarized with DaeCoat™ 515, bonded with DaeCoat™ 350 (tunable adhesion force) to a carrier, and processed through the customer's line. De-bonding occurs by capillary driven penetration into the bond line to effect separation while the device wafer is supported onto a taped film frame. A tape-safe chemistry, DaeClean™ 300, is used in a simple wet bench tool offering low cost and throughput defined by the size of the cassette and tank (Fig. 11).

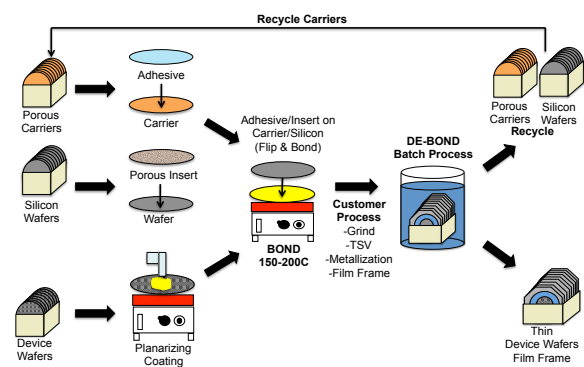


Fig. 11. DaeBond 3D™ technology flow.

Carrier de-bonding occurs in Tank 1 by liquid penetration to break the edge seal and migrates swiftly through the porous coating until saturation causes a drop in adhesion. Cassettes of film frames

holding device wafers proceed to tank 2 for final washing (Figs. 12 & 13).

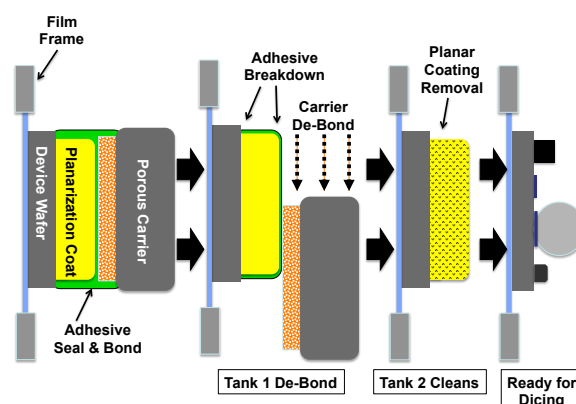


Fig. 12. Step-wise carrier de-bond & wafer cleans.

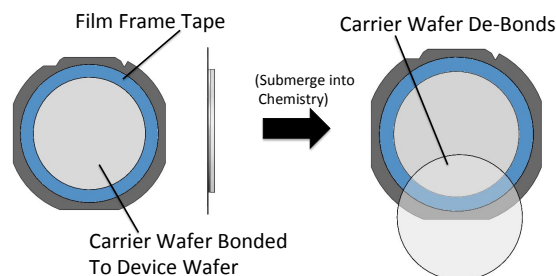


Fig. 13. Carrier de-bond from the taped film frame.

II. EXPERIMENTAL

A. Materials

For process demonstration and testing, remanufactured silicon substrates at diameters of 100-200 mm (4-8") of known crystal orientation and thickness (1-0-0, ~525 μm; Wollemi Technical, Inc. Taiwan, www.wollemi.com.tw). Materials used include: a) DaeCoat™ 515 (planarizing coating), b) DaeCoat™ 350 (adhesive w/tunable force), and c) DaeClean™ 300 (cleaner) [15]. Process chemistries include: TMAH (0.26N), isopropanol (IPA), n-methylpyrrolidone (NMP), various dilute mineral acids, and sulfuric acid copper plating bath. Tape products for film frame applications include: Lintec and Nitto-Denko.

B. Equipment

Coatings are produced on a Brewer Science, Inc. CB-100 spin-coater, while spray and encapsulation uses custom tooling designed at Daetec. Metrology data is generated by a XP-1 stylus profiler, AFP-200 atomic force profiler, and a Xi-100 optical profiler [16]. Where applicable, equipment settings include a 5 mg stylus load, minimum 4 mm distance, and speed of 0.5 mm/sec. Bonding and de-bonding equipment is designed at Daetec for radiation and thermal cure.

III. RESULTS

A. Thermal Resistance

Temperature resistance is measured by several

methods, including material degradation and performance by adhesion force. Thermal outgas measurements are conducted by laboratory modified TGA methods on both the porous coating and adhesive. Resistance to 450°C in an inert environment has been confirmed (Fig. 14).

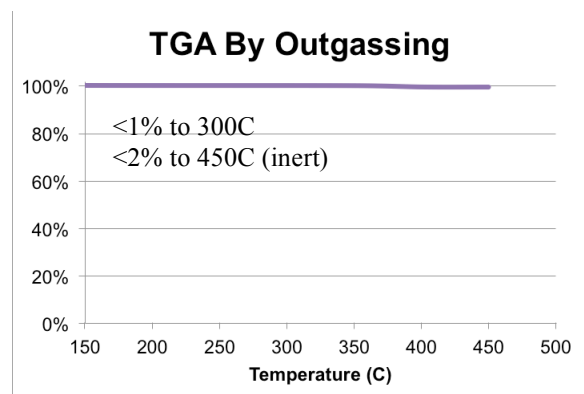


Fig. 14. Thermal outgas measurement of adhesive.

Adhesive force is measured by a peel mechanism. The system set-up using a digital load cell becomes a physics problem with the measured adhesion force must exceed the material adhesion yet be lower than the product's tensile strength (Fig. 15). Multiple cycles exposed to 350°C are measured (Fig. 16).

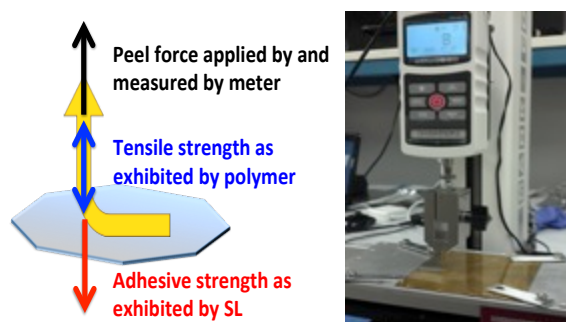


Fig. 15. Adhesive force measurement set-up.

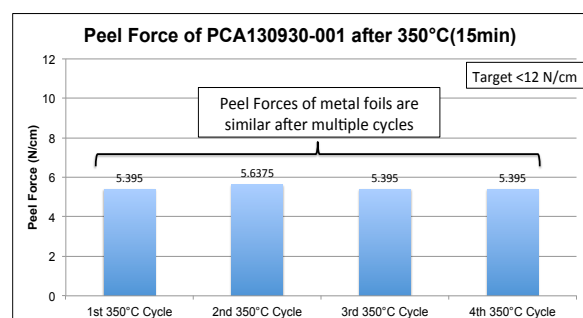


Fig. 16. Adhesive force measured separately for multiple thermal exposures to 350°C.

B. Fluid Capillary Migration

Daetec uses several monitors to control the quality of the porous coating, including thickness, surface texture (roughness), and wick height (liquid travel

distance). Daetec has developed methods to measure material transport through the coating (Fig. 17).

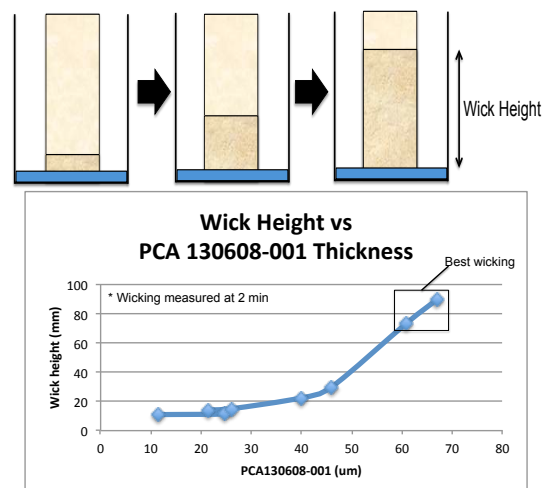


Fig. 17. Liquid travel through porous coating as wick height (above) and its relation to thickness (below).

C. De-bond Performance

Carrier de-bond from film frame supported wafers is conducted using a range of fixtures designed by Daetec. The wafer stack is affixed via the device wafer to a taped film frame. The bonded film frame is immersed into a liquid that initiates the de-bond process (Fig. 18).

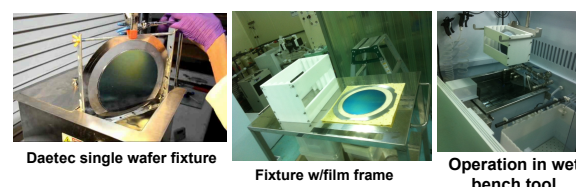


Fig. 18. Testing de-bond with mounted device wafers on film frames occur on a single-frame and a Teflon® multi-frame fixture in a wet bench.

Extended time and temperature tests are performed with several chemistries including DaeClean™ 300. Although some effects were observed, the majority survived, including several common acrylic tapes from leading suppliers (e.g. Furukawa, Lintec, and Nitto-Denko).

V. CONCLUSIONS

This paper introduces the use of several temporary bonding products for handling thin substrates in semiconductor and display manufacturing. Properties as thermal resistance, de-bond conditions, and tool requirements enable a manufactured product to be achieved. Capturing these and other properties surrounding temporary bonding combine to achieve high value thin wafer support. A new temporary bonding system, DaeBond 3D™, is presented here to provide options for batch de-bonding.

ACKNOWLEDGMENT

The authors would like to thank the staff at Daetec for making this work possible.

REFERENCES

- [1] A. Palesko, C. Palesko, Cost Comparison of Temporary Bond and Debond Methods for Thin Wafer Handling, *IMAPS 10th Intl. Conf. and Exhib. On Device Pkg*, March 10-13 (2014).
- [2] Semicon-West, San Francisco, CA, SEMI/panel discussion, July, 2013.
(http://www.semiconwest.org/sites/semiconwest.org/files/docs/SW.ShowDaily13.Day3_FP_low.pdf).
- [3] F. Livesey, Defining High Value Manufacturing, *Report by Dept. of Trade and Ind. (DTI) and Conf. of Brit. Ind. (CBI)*, January 2006.
- [4] U.S. Patent No. 7,678,861, J. Moore and M. Fowler, March 16, 2010.
- [5] J. Moore, et al., Thermal Resistant Polymers for Microelectronic Applications, *Society for the Advancement of Materials and Process Engineering (SAMPE) Conference*, Long Beach, CA, May (2013).
- [6] D. Mould, and J. Moore, A New Alternative for Temporary Wafer Mounting, *Proceedings for GaAs MANTECH*, April 2002, pp.109-112.
- [7] J. Moore, A. Smith, D. Nguyen, and S. Kulkarni, High Temperature Resistant Adhesive for Wafer Thinning and Backside Processing, 2004 *Proceedings for GaAs MANTECH*, May 2004, pp. 175-178.
- [8] A. Smith, J. Moore, and B. Hosse, A Chemical and Thermal Resistant Wafer Bonding Adhesive for Simplifying Wafer Backside Processing, *Proceedings for GaAs MANTECH*, April 2006, pp.269-271.
- [9] U.S. Patent Applications 2009/0017248 A1 (2009), *Larson et al.*; 2009/0017323 A1 (2009), *Webb et al.*; and International Application WO 2008/008931 A1 (2008), *Webb et al.*
- [10] J. Pettit, and J. Moore, Extreme Temporary Coatings and Adhesives for High Thermal, Low Pressure, and Low Stress 3D Processing, *IMAPS Proceedings for Microelectronics*, Long Beach, CA, October (2011).
- [11] J. Pettit, and J. Moore, Thermal Resistant Coatings Using PBI Resin, *Society for the Advancement of Materials and Process Engineering (SAMPE) Conference*, Baltimore, MD, May (2012).
- [12] Polybenzimidazole (PBI) polymer is exclusively available in a variety of forms, including powder, solutions and hybrid polymer systems from PBI Performance Products, Inc., www.pbipproducts.com.
- [13] S. Dhoot, B. Freeman, and M. Stewart, *Barrier Polymers*, Ency. Poly. Sci. Tech., March (2002).
- [14] K.C. Su, H.H. Lu, S.H. Chen, C.D. Tsai, Y.C. Chou, b W.J. Wu, G.Q. Wu, and J.C. Moore, A Novel Water-Washable Coating for Avoiding Contamination During Dry Laser Dicing Operations, *Proceedings for GaAs ManTech Conference*, pp. 317-320, May 2007.
- [15] Spin coatings, adhesives, encapsulants, cleaners, equipment, and processing designs utilizing a wide Daetec.IMAPS.SD.2014.r1.docx

range of cure approaches including evaporative, photo, and thermal are from Daetec, LLC, www.daetec.com.

[16] Series XP, AFP, and Xi, are contact and non-contact profilometers as produced by Ambios Technology, Inc., www.ambiosotech.com.